

VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution, Affiliated to Anna University Chennai)



COLLEGE VISION

To impart value based education in Engineering and Technology to empower young women to meet the societal exigency with a global outlook.

COLLEGE MISSION

- To provide holistic education through innovative teaching-learning practices
- To instill self confidence among rural students by supplementing with cocurricular and extra-curricular activities
- To inculcate the spirit of innovation through training, research and development
- To provide industrial exposure to meet the global challenges
- To create an environment for continual progress through lifelong learning

DEPARTMENT VISION

To Produce Innovative, Creative, Ethical and Socially responsible Electronics and Communication women engineers to meet the global challenges

DEPARTMENT MISSION

- To create a unique learning environment in Electronics and Communication Engineering to mould a strong engineer with professional ethics
- > To provide practical exposure to compete in the global market
- Fostering culture of innovation, research and lifelong learning

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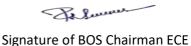




M.E. VLSI DESIGN <u>Regulation 2023</u> CHOICE BASED CREDIT SYSTEM

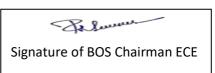
PROGRAMME EDUCATIONAL OBJECTIVES (PEOs)

- PEO I. To acquire a background in Basic science and Mathematics and ability to use these tools in VLSI Design.
- PEO II. Teach students to understand the principles involved in the latest software required for designing and critically analyzing electronic systems relevant to industry and society.
- PEO III. To attain the qualities of professional leadership to deliver effectively in a multi-disciplinary team and domains
- PEO IV. Mould students to be able to communicate efficiently
- PEO V. Motivate students to take up socially relevant and challenging projects and propose innovative solution to problems for the benefit of society.



PROGRAMME OUTCOMES (POs)

- PO 1. Apply knowledge of Mathematics, Science, Engineering fundamentals and an Engineering specialization to the conceptualization of Engineering models.
- PO 2. Identify, formulate, research literature and solve complex Electronics and communication engineering problems reaching substantiated conclusions using first principles of Mathematics and Engineering sciences.
- PO 3. Design solutions for complex Electronics and Communication Engineering problems and design systems, components or processes that meet specified needs with appropriate consideration for public health and safety, cultural, societal, and environmental considerations.
- PO 4. Conduct investigations of complex problems including design of experiments, analysis and interpretation of data, and synthesis of information to provide valid conclusions.
- PO 5. Create, select and apply appropriate techniques, resources, and modern Engineering tools, including prediction and modeling, to complex Electronics and Communication Engineering activities, with an understanding of the limitations.
- PO 6. Function effectively as an individual, and as a member or leader in diverse teams and in multi disciplinary settings.
- PO 7. Communicate effectively on complex Electronics and Communication Engineering activities with the Engineering community and with society at large, such as being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
- PO 8. Demonstrate understanding of the societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to Engineering practice.



- PO 9. Understand and commit to professional ethics and responsibilities and norms of engineering practice.
- PO 10. Understand the impact of engineering solutions in a societal context and demonstrate knowledge of and need for sustainable development.
- PO 11. Demonstrate a knowledge and understanding of management and business practices, such as risk and change management, and understand their limitations.
- PO 12. Recognize the need for, and have the ability to engage in independent and lifelong learning.

PROGRAM SPECIFIC OUTCOMES (PSOs):

At the end of this program, graduate will be able to:

PSO 1: Comprehend the basic concepts of VLSI Design and apply them in the day to day life to design and execute complete engineering systems.

PSO 2: Design, verify and validate VLSI functional elements for numerous applications including signal processing, communications, computer networks.

PSO 3: Demonstrate the intellectual level with peer engineers and others to work together to arrive at a cost-effective, appropriate solution for various problems.

MAPPING OF PROGRAMME EDUCATIONAL OBJECTIVES (PEO_S) WITH PROGRAMME OUTCOMES (PO_S)

A broad relation between the programme educational objective and the outcomes is given in the following table

PROGRAMME		PROGRAMME OUTCOMES										
EDUCATIONAL OBJECTIVES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
PEO 1	~	✓					\checkmark					
PEO 2			✓	✓	~							✓
PEO 3				✓		✓						
PEO 4						✓				✓	✓	
PEO 5						✓	✓	✓	✓	~	~	✓

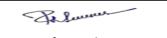
SEM	Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO 9	PO10	PO11	PO12
	Applied Mathematics	~	~	~		~							
Ι	CMOS Analog Semiconductor Design	~	~	~		~							

	VLSI Digital Signal	~	✓	~		✓							
	Processing Professional Elective – I												
	Professional Elective – II												
	Audit Course I												
	VLSI System Laboratory-I	~	✓			✓			~	✓	✓		
	Electronic Design Automation Laboratory	~	~			~			~	~	~		
	Low Power VLSI Design	~	~	~		\checkmark							
	Testing and Verification of VLSI Circuits	~	~	~		\checkmark							
	VLSI for Wireless Communication	~	~	~		~							
	Professional Elective – III												
II	Professional Elective – IV Audit Course II												
	VLSI System Laboratory-II	~	~			~			~	~	~		
	VLSI Design Verification and Testing Laboratory	~	~			~			~	~	~		
	Mini Project-I	~	\checkmark			\checkmark			~	\checkmark	~		
	Professional Elective – V												
ш	Open Elective - I												
	Dissertation Phase -I	~	~	~	~	~	~	~	~	\checkmark	~	~	~
IV	Dissertation Phase – II	~	~	~	~	\checkmark	\checkmark	~	~	~	~	~	~

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Q		VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution Affiliated to Anna University Chennai) Elayampalayam, Tiruchengode – 637 205											
Programme	M.E.	Programme Code			205		Regulat	ion	2023				
Department		IGN / ELECTRO NICATION ENGI					ster	ster I					
	(Applicable t	o the students admi	CURRICU tted from tl		lemic ye	ar 2023	-2024 on	wards))				
Course Code	Cou	ırse Name	Category	Per	riods / W	eek	Credit	Max	kimum N	Aarks			
			89	L	Т	Р	C	CA	ESE	Total			
	THEORY												
P23MA102	Applied Ma	Applied MathematicsFC300340											
P23VD101	CMOS Ana Semicondu	alog ctor Design	PCC	3	0	0	3	40	60	100			
P23VD102	VLSI Digit Processing	al Signal	PCC	3	0	0	3	40	60	100			
	Professional	Elective – I	PEC	3	0	0	3	40	60	100			
	Professional	Elective – II	PEC	3	0	0	3	40	60	100			
	Audit Course	e-I	AC	2	0	0	0	100	-	100			
			PRACTI	CAL									
P23VD103	VLSI Syste	VLSI System Laboratory-IPCC00426040100											
P23VD104	Electronic I Laboratory	Design Automation	PCC	0	0	4	2	60	40	100			
					Total C	redits	19	420	380	800			

PCC – Professional Core Course, PEC – Professional Elective Course, PAC- Program Audit Course, FC-Foundational Course, CA - Continuous Assessment, ESE - End Semester Examination



Q		NANDHA COLLE onomous Institution Elayampalay	Affiliated t	o Ann	a Unive	ersity C			UVRheinland CERTIFIED U Stotkeinis	
Programme	M.E.	Programme Code			205		Regulat	tion	2023	;
Department		IGN / ELECTRON IICATION ENGIN		1			Seme	ster	Π	
	(Applicable t	o the students admit	CURRICU		emic ye	nwards)				
Course Code	Cou	rse Name	Category	Per	iods / W	/eek	Credit	Maxi	mum Ma	arks
	000		Cutogory	L	Т	Р	С	CA	ESE	Tot al
			THEOR	Y						
P23VD205	Low Power	VLSI Design	PCC	3	0	0	3	40	60	100
P23VD206	Testing and VLSI Circui	Verification of ts	PCC	3	0	0	3	40	60	100
P23VD207	VLSI for Wir Communicati		PCC	3	0	0	3	40	60	100
	Professional	Elective – III	PEC	3	0	0	3	40	60	100
	Professional	Elective – IV	PEC	3	0	0	3	40	60	100
	Audit Cours	e-II	AC	2	0	0	0	100	-	100
			PRACTIC	CAL						
P23VD208	VLSI Syste	m Laboratory-II	PCC	0	0	4	2	60	40	100
P23VD209	VLSI Desig Testing Lab	n Verification and poratory	PCC	0	0	4	2	60	40	100
P23VD210	Mini Projec	t-I	EEC	0	0	4	2	100	-	100
]	Fotal C	redits	21	460	440	900

PCC – Professional Core Course, PEC – Professional Elective Course, PAC- Program Audit Course,

CA - Continuous Assessment, ESE - End Semester Examination

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		ANDHA COLLEG tonomous Institutio Elayampala	n Affiliated	to Ar	na Univ	versity C			UVRheinland CERTIFIED	N01:2015			
Programme	M.E.	Programme Code			205		Regula	tion	2023				
Department		IGN / ELECTRO NICATION ENGI					Semester		ter III				
	Applicable to	CURRICULUM pplicable to the students admitted from the academic year 2023-2024 onwards)											
Course Code	Cou	Course Name Category Periods / Week Credit Maximum Marks											
			89	L	Т	Р	С	CA	ESE	Total			
			THEOR	RY									
	Professiona	al Elective –V	PEC	3	0	0	3	40	60	100			
	Open Electi	ive – I	OEC	3	0	0	3	40	60	100			
			PRACTIC	CAL									
P23VD311	Dissertation	n Phase –I	EEC	0	0	16	8	60	40	100			
					Total C	redits	14	140	160	300			

PEC – Professional Elective Course, OEC- Open Elective Course, EEC – Employability Enhancement Course CA - Continuous Assessment, ESE - End Semester Examination

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9	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution Affiliated to Anna University Chennai) Elayampalayam, Tiruchengode – 637 205 Image: Constraint of the second s												
Programme	M.E.												
Department		SI DESIGN / ELECTRONICS AND MMUNICATION ENGINEERING Semester IV											
	CURRICULUM (Applicable to the students admitted from the academic year 2023-2024 onwards)												
Course Code	Cours	se Name	Category	Perio	ds / W	Veek	Credit	Max	imum N	Aarks			
			Cuttegory	L	Т	Р	С	CA	ESE	Total			
			PRACT	ICAL									
P23VD412	Dissertation	Phase – II	EEC	0	0	32	16	60	40	100			
				Т	otal (Credits	16	60	40	100			

 $\mbox{EEC}-\mbox{Employability}$ Enhancement Course, CA - Continuous Assessment, \mbox{ESE} - End Semester Examination

Cumulative Course Credits -70

Course Code	Course Name	Category	Peri	iods / We	ek	Credit	Max	imum N	Marks
Course Code	Course Maine	Category	L	Т	Р	С	CA	ESE	Total
P23VD101	CMOS Analog Semiconductor Design	PCC	3	0	0	3	40	60	100
P23VD102	VLSI Digital Signal Processing	PCC	3	0	0	3	40	60	100
P23VD103	VLSI System Laboratory-I	PCC	0	0	4	2	60	40	100
P23VD104	Electronic Design Automation Laboratory	PCC	0	0	4	2	60	40	100
P23VD205	Low Power VLSI Design	PCC	3	0	0	3	40	60	100
P23VD206	Testing and Verification of VLSI Circuits	PCC	3	0	0	3	40	60	100
P23VD207	VLSI for Wireless Communication	PCC	3	0	0	3	40	60	100
P23VD208	VLSI System Laboratory-II	PCC	0	0	4	2	60	40	100
P23VD209	VLSI Design Verification and Testing Laboratory	PCC	0	0	4	2	60	40	100

PROFESSIONAL CORE COURSES (PCC)

ENHANCED EMPLOYABILITY COURSES (EEC)

Course	Course Name	Catagory	Per	iods / Wo	eek	Credit	Maxin	num Ma	rks
Code	Course mame	Category	L	Т	Р	С	CA	ESE	Total
P23VD210	Mini Project-I	EEC	0	0	4	2	60	40	100
P23VD311	Dissertation Phase -I	EEC	0	0	16	8	60	40	100
P23VD412	Dissertation Phase – II	EEC	0	0	32	16	60	40	100

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FOUNDATION COURSE (FC)

Course	Course Name	Category	Peri	iods / V	Veek	Credit	Credit Maximum Marks		
Code	Course Maine	Category	L	Т	Р	С	CA	ESE	Total
P23MA102	Applied Mathematics	FC	3	0	0	3	40	60	100

PROFESSIONAL ELECTIVE - I

Course code	Course Name	Category	L	Т	Р	С	CA	ESE	Total
P23VDE01	Embedded System Design	PEC	3	0	0	3	40	60	100
P23VDE02	Physics of MOS Transistors	PEC	3	0	0	3	40	60	100
P23VDE03	Foundations of VLSI CAD	PEC	3	0	0	3	40	60	100
P23VDE04	HDL with System Modeling	PEC	3	0	0	3	40	60	100

PROFESSIONAL ELECTIVE - II

Course code	Course Name	Category	L	Т	Р	С	CA	ESE	Total
P23VDE05	Introduction to MEMS	PEC	3	0	0	3	40	60	100
P23VDE06	Multimedia Compression Techniques	PEC	3	0	0	3	40	60	100
P23VDE07	Semiconductor Memory Design	PEC	3	0	0	3	40	60	100
P23VDE08	System on Chip Design	PEC	3	0	0	3	40	60	100

PROFESSIONAL ELECTIVE – III

Course code	Course Name	Category	L	Т	Р	С	CA	ESE	Total
P23VDE09	Hardware Design Verification Techniques	PEC	3	0	0	3	40	60	100
P23VDE10	RF Microelectronics Chip Design	PEC	3	0	0	3	40	60	100
P23VDE11	Mixed Signal VLSI Design	PEC	3	0	0	3	40	60	100
P23VDE12	Nano Electronics	PEC	3	0	0	3	40	60	100

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PROFESSIONAL ELECTIVE - IV

Course code	Course Name	Category	L	Т	Р	С	CA	ESE	Total
P23VDE13	Processors and Embedded Controllers	PEC	3	0	0	3	40	60	100
P23VDE14	Digital System Design With FPGA	PEC	3	0	0	3	40	60	100
P23VDE15	Speech and Audio Signal Processing	PEC	3	0	0	3	40	60	100
P23VDE16	Internet of Things And Applications	PEC	3	0	0	3	40	60	100

PROFESSIONAL ELECTIVE - V

Course code	Course Name	Category	L	Т	Р	С	CA	ESE	Total
P23VDE17	Soft Computing	PEC	3	0	0	3	40	60	100
P23VDE18	Networks on Chip	PEC	3	0	0	3	40	60	100
P23VDE19	ARM processor and architecture	PEC	3	0	0	3	40	60	100
P23VDE20	Wireless Adhoc and Sensor Networks	PEC	3	0	0	3	40	60	100

OPEN ELECTIVE OFFERED TO OTHER DEPARTMENTS

Course code	Course Name	Category	L	Т	Р	С	CA	ESE	Total
P23VDOE1	Micro sensors and MEMS	OEC	3	0	0	3	40	60	100
P23VDOE2	Basics of VLSI	OEC	3	0	0	3	40	60	100
P23VDOE3	Communication Busses and Interfaces	OEC	3	0	0	3	40	60	100

OPEN ELECTIVE (EEE)

Course code	Course Name	Category	L	Т	Р	С	CA	ESE	Total
P23PSOE1	Industrial Safety	OEC	3	0	0	3	40	60	100
P23PSOE2	Energy storage Technologies	OEC	3	0	0	3	40	60	100
P23PSOE3	Energy Management and Auditing	OEC	3	0	0	3	40	60	100
P23PSOE4	Electrical Circuit design for Hazardous in Industries	OEC	3	0	0	3	40	60	100

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AUDIT COURSES (AC)

Course	Course Name	Cotocom	Per	iods / W	eek	Credit	Maxin	num Ma	arks
Code	Course Manie	Category	L	Т	Р	С	CA	ESE	Total
		AUDIT	COU	RSE-I					
P23AC001	Research Process and Methodologies	AC	2	0	0	0	100	0	100
P23AC002	Pedagogy Studies	AC	2	0	0	0	100	0	100
P23AC003	Disaster Management	AC	2	0	0	0	100	0	100
P23AC004	Value Education	AC	2	0	0	0	100	0	100
P23AC005	Constitution of India	AC	2	0	0	0	100	0	100
		AUDIT	COU	RSE-II	1		L	1	
P23AC006	English for Research Paper Writing	AC	2	0	0	0	100	0	100
P23AC007	Personality Development through Life Enlightenment	AC	2	0	0	0	100	0	100
P23AC008	Universal Human Values	AC	2	0	0	0	100	0	100
P23AC009	Online Course	AC	2	0	0	0	100	0	100

S.No.	Course Components	Cr	edits per :	semeste	er	Total number of credits for each
		Ι	II	III	IV	component
1	Foundational Course (FC)	3	-	-	-	3
2	Programme Core Courses (PCC)	10	13	_	_	23
3	Professional Elective Course (PEC)	6	6	3	-	15
4	Open Electives (OE)	-	-	3	-	3
5	Employability Enhancing Courses (EEC)	-	2	8	16	26
6	Programme Audit Course (PAC)	-	-	-	-	_
Total (Credits	20	21	14	16	70

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	VLSI	Desig	n	1102	Stamme				200		Seme			I	
ode		Cour	se Nar	ne		Periods			Credit				um Ma		
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PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3	
3	2	1		1					-			2			1
3	-	1	1	1				_	_			2			4
-		1	1	1											-
			1	1				_		1					-
ntinuou	t Metho	ods sment '		I & III		1					I	2	1]
	PO 1 3 3 3 3 3 3 3 ssment	At the CO1: sample CO2: in the f CO3: probab CO4: CO5: Loadir tes - (3/2/1 indic PO1 PO2 3 2 3 2 3 2 3 2 3 2 3 2 3 2 3 2 3 2 3 2 3 2 3 2 3 2 3 2 3 2 3 3 2 3 2 3 2 3 2 3 <	 This nume probl To a plays Ident Ident Ident Ident Ident Ident Ident Ident Oter At the end of CO1: Apply samples in re CO2: Apply in the field of CO3: App probability/st CO4: Incorpo CO5: Recogr Loading methetics - 	 This course numerical r problems oc To acquaint plays an imp Identify and Identify the Potentially u At the end of the course course in real life p CO1: Apply the cost samples in real life p CO2: Apply the bass in the field of agricut CO3: Apply a probability/statistica CO4: Incorporate Trice CO5: Recognize Dy Loading method. tes - 	 This course aims numerical method problems occurring To acquaint the kr plays an important Identify and demories in the formul Potentially understated at the end of the course, the CO1: Apply the concept samples in real life problem CO2: Apply the basic concerns in the field of agriculture. CO3: Apply appropring probability/statistical concerns CO4: Incorporate Transport CO5: Recognize Dynamic Loading method. tes - CO 1 PO 2 PO 3 PO 4 PO 5 3 2 1 1 	 This course aims at provnumerical methods and problems occurring in eng To acquaint the knowledge plays an important role in Identify and demonstrate set Identify the formulation are Potentially understand for At the end of the course, the student CO1: Apply the concept of test samples in real life problems. CO2: Apply the basic concepts of in the field of agriculture. CO3: Apply appropriate probability/statistical concepts. CO4: Incorporate Transportation are CO5: Recognize Dynamic program Loading method. tes - 	numerical methods and give p problems occurring in engineerin • To acquaint the knowledge of te plays an important role in real life • Identify and demonstrate suitable • Identify the formulation and grap • Potentially understand forward and At the end of the course, the student should CO1: Apply the concept of testing of samples in real life problems. CO2: Apply the basic concepts of classifi in the field of agriculture. CO3: Apply appropriate moder probability/statistical concepts. CO4: Incorporate Transportation and Ass CO5: Recognize Dynamic programming Loading method. tes - CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, Programme Outcomes PO1 PO2 PO3 PO4 PO5 PO6 PO7 3 2 1 1 1 1 3 2 1 1 1 1 3 2 1 1 1 1 3 2 1 1 <td< td=""><td>This course aims at providing the mumerical methods and give procedu problems occurring in engineering and To acquaint the knowledge of testing plays an important role in real life prob Identify and demonstrate suitable samp Identify the formulation and graphical s Potentially understand forward and bac At the end of the course, the student should be abl CO1: Apply the concept of testing of hypor samples in real life problems. CO2: Apply the basic concepts of classification in the field of agriculture. CO3: Apply appropriate modern to probability/statistical concepts. CO4: Incorporate Transportation and Assignme CO5: Recognize Dynamic programming applic Loading method. tes - CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Ma Programme Outcomes (POs) PO 1 PO 2 PO 3 PO 4 PO 5 PO 6 PO 7 PO 8 3 2 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1</td><td>This course aims at providing the necessar numerical methods and give procedures for problems occurring in engineering and technol To acquaint the knowledge of testing of hyp plays an important role in real life problems. Identify and demonstrate suitable sampling and Identify the formulation and graphical solution Potentially understand forward and backward and At the end of the course, the student should be able to CO1: Apply the concept of testing of hypothesis f samples in real life problems. CO2: Apply the basic concepts of classifications of de in the field of agriculture. CO3: Apply appropriate modern technoloc probability/statistical concepts. CO4: Incorporate Transportation and Assignment prob CO5: Recognize Dynamic programming applications to Loading method. tes - CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 Programme Outcomes (POs) Po 1 PO 2 PO 3 PO 4 PO 5 PO 6 PO 7 PO 8 PO 9 3 2 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1</td><td>This course aims at providing the necessary basic numerical methods and give procedures for solvir problems occurring in engineering and technology. To acquaint the knowledge of testing of hypothesis is plays an important role in real life problems. Identify and demonstrate suitable sampling and data complex and graphical solution of linear elements. Identify the formulation and graphical solution of linear events of the end of the course, the student should be able to CO1: Apply the concept of testing of hypothesis for smal samples in real life problems. CO2: Apply the concept of testing of hypothesis for smal samples in real life problems. CO2: Apply the basic concepts of classifications of design of in the field of agriculture. CO3: Apply appropriate modern technology to probability/statistical concepts. CO4: Incorporate Transportation and Assignment problems. CO5: Recognize Dynamic programming applications using Loading method. tes - CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak Programme Outcomes (POs) Po1 PO2 PO3 PO4 PO5 PO6 PO7 PO8 PO9 PO 10 3 2 1 1 1 1 1</td><td>This course aims at providing the necessary basic conc numerical methods and give procedures for solving me problems occurring in engineering and technology. To acquain the knowledge of testing of hypothesis for se- plays an important role in real life problems. Identify and demonstrate suitable sampling and data collect I dentify the formulation and graphical solution of linear pro- Potentially understand forward and backward recursion. At the end of the course, the student should be able to CO1: Apply the concept of testing of hypothesis for small and samples in real life problems. CO2: Apply the basic concepts of classifications of design of experi- in the field of agriculture. CO3: Apply appropriate modern technology to or probability/statistical concepts. CO4: Incorporate Transportation and Assignment problems. CO5: Recognize Dynamic programming applications using Loading method. tes - CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak Programme Outcomes (POs) PO1 PO2 PO3 PO4 PO5 PO6 PO7 PO8 PO9 PO PO 10 11 1 1</td><td>This course aims at providing the necessary basic concepts on numerical methods and give procedures for solving numerical problems occurring in engineering and technology. To acquaint the knowledge of testing of hypothesis for small a plays an important role in real life problems. Identify and demonstrate suitable sampling and data collection providentiation of the formulation and graphical solution of linear programm. Potentially understand forward and backward recursion. At the end of the course, the student should be able to CO1: Apply the concept of testing of hypothesis for small and larg samples in real life problems. CO2: Apply the basic concepts of classifications of design of experiment in the field of agriculture. CO3: Apply appropriate modern technology to explor probability/statistical concepts. CO4: Incorporate Transportation and Assignment problems. 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Unit –	- I	TESTING OF HYPOTHESIS	Periods	9
		tions - Estimation of parameters - Statistical hypothesis - Lar		
		ngle mean and difference of means -Tests based on t, Chi-squ		ibutions for mean
	<u> </u>	ortion - Contingency table (test for independent) - Goodness of fi		
Unit -		DESIGN OF EXPERIMENTS	Periods	9
One way a design -2^2		way classifications - Completely randomized design – Randor al design.	mized block des	ign – Latin squar
Unit –	III	ESTIMATION THEORY	Periods	9
		tions, point estimation, unbiasedness, consistency, maximum	likelihood estin	nation, Confidenc
		neter in one sample from normal population.		
Unit -		LINEAR PROGRAMMING	Periods	9
		hical solution-Simplex Method -Transportation and Assignment		
Unit -		DYNAMIC PROGRAMMING	Periods	<u>9</u>
		ming-principle of optimality-forward and backward recursion of dimensionality.	I-DP Applicatio	ns (Cargo loadin
			Total Periods	45
Text Book				
1.		las.C; Montgomery, 'Applied Statistics and Probability for Engine, Wiley, 2017.	ineers', 6 th Editio	on, Wiley Student
1. 2.	Editio			-
2.	Editio Hamo s	on, Wiley, 2017. dy A. Taha., 'Operations Research: An Introduction', 9 th Edition	, Pearson New I	Delhi, 2014.
2.	Edition Hamo S Richa	on, Wiley, 2017.	, Pearson New I	Delhi, 2014.
2. Reference	Edition Hamo S Richa Pears	on, Wiley, 2017. dy A. Taha., 'Operations Research: An Introduction', 9 th Edition ard. A. Johnson , Irwin Miller,' Probability And Statistics For En	, Pearson New I	Delhi, 2014.
2. References	Edition Hamo s Richa Pears Kalya	on, Wiley, 2017. dy A. Taha., 'Operations Research: An Introduction', 9 th Edition ard. A. Johnson , Irwin Miller,' Probability And Statistics For En on Education, Delhi,2020.	, Pearson New I gineers', 8 th Edit	Delhi, 2014.
2. Reference: 1. 2.	Edition Hamo S Richa Pears Kalya Kanti Rona	bn, Wiley, 2017. dy A. Taha., 'Operations Research: An Introduction', 9 th Edition ard. A. Johnson , Irwin Miller,' Probability And Statistics For En on Education, Delhi,2020. anmoy Deb., 'Optimization For Engineering Design', Phi, 2004.	gineers', 8 th Edit gineers', 8 th Edit	Delhi, 2014. tion, rning, 2013.
2. Reference 1. 2. 3.	Edition Hamo S Richa Pears Kalya Kanti Rona Pears	 bn, Wiley, 2017. dy A. Taha., 'Operations Research: An Introduction', 9th Edition ard. A. Johnson , Irwin Miller,' Probability And Statistics For En on Education, Delhi,2020. anmoy Deb., 'Optimization For Engineering Design', Phi, 2004. B. Datta., 'Mathematical Methods Of Science And Engineering ld E.Walpole & Raymond H.Myers 'Probability And Statistics I 	gineers', 8 th Edit gineers', 8 th Edit g', Cengage Lear For Engineers An	Delhi, 2014. tion, ming, 2013. nd Scitintists',
2. Reference 1. 2. 3. 4. 5.	Edition Hamo Richa Pears Kalya Kanti Rona Pears Kotha	 bn, Wiley, 2017. dy A. Taha., 'Operations Research: An Introduction', 9th Edition ard. A. Johnson , Irwin Miller,' Probability And Statistics For En on Education, Delhi,2020. anmoy Deb., 'Optimization For Engineering Design', Phi, 2004. B. Datta., 'Mathematical Methods Of Science And Engineering ld E.Walpole & Raymond H.Myers 'Probability And Statistics For Engineering ld E.Walpole & Raymond H.Myers 'Probability And Statistics For Engineering. 	gineers', 8 th Edit gineers', 8 th Edit g', Cengage Lear For Engineers An	Delhi, 2014. tion, ming, 2013. nd Scitintists',
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2. References 1. 2. 3. 4. 5. E-Resource	Edition Hamo Richa Pears Kalya Kanti Rona Pears Kotha es <i>https:</i>	 bn, Wiley, 2017. dy A. Taha., 'Operations Research: An Introduction', 9th Edition ard. A. Johnson , Irwin Miller,' Probability And Statistics For Encon Education, Delhi,2020. anmoy Deb., 'Optimization For Engineering Design', Phi, 2004. B. Datta., 'Mathematical Methods Of Science And Engineering Id E.Walpole & Raymond H.Myers 'Probability And Statistics I on Education, Delhi, 9th Edition, 2014. ari.C.R., 'An Introduction To Operational Research' 3rd Edition, 	gineers', 8 th Edit gineers', 8 th Edit g', Cengage Lear For Engineers An	Delhi, 2014. tion, ming, 2013. nd Scitintists',

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COs]	Program	me Out	comes ((POs)					PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO	9 PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
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		ransistor (or	nputer Simulation
mouch,	g - Other Model Parameters, Small-Signal Model for the MOS T Sub-threshold MOS Model. IC Packaging: Types and Modeling		
	Modeling- Stress Modeling-Package Simulation- Flip-Chip Package		achage modeling
Unit -		Periods	9
The Cu	rrent Mirror: The Cascode Connection-Sensitivity Analysis-T	emperature A	Analysis-Transient
Response	e-Layout of the Simple Current Mirror-matching in MOSFET	Γ Mirrors-Rei	ferences: Voltage
Dividers	- Current Source Self Biasing: Threshold Voltage Referenced S	elf-Biasing- H	Band gap Voltage
Referenc	es-Beta Multiplier Referenced Self Biasing.		
Unit –	III AMPLIFIERS	Periods	9
Feedback Topologi Amplifie	rs: Gate-Drain Connected Loads-Current Source Loads-Noise Amplifiers: Properties of Negative Feedback on Amplifier les- Voltage Amplifier- Transimpedance Amplifier – Transcond r-Output Amplifier-Cascode Amplifiers-Source Follower-Vo	Design-Recog	gnizing Feedback plifier – Current
Uperation	nal Amplifier- Differential Amplifier.IVDATA CONVERTERS AND ARCHITECTURES	Periods	9
	Versus Discrete Time Signals- S/H Characteristics- Mixed		
Two-Step	Charge Scaling DACs-Cyclic DAC- Pipeline DAC- ADC Specific p Flash ADC-Pipeline ADC-Integrating ADC-Successive Appr		
ADC.			DC-Oversampning
Unit -	-V COMPARATORS	Periods	9
Unit - Characte		Periods ther Open-Lo	9
Unit - Characte	- V COMPARATORS rization of Comparator, Two-Stage, Open-Loop Comparators, O ng the Performance of Open-Loop Comparators, Discrete-Time Com	Periods ther Open-Lo	9 op Comparators,
Unit - Characte	- V COMPARATORS rization of Comparator, Two-Stage, Open-Loop Comparators, O ng the Performance of Open-Loop Comparators, Discrete-Time Com	Periods ther Open-Lo nparators.	9 op Comparators,
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Unit - Characte Improvin	V COMPARATORS rization of Comparator, Two-Stage, Open-Loop Comparators, O ag the Performance of Open-Loop Comparators, Discrete-Time Com Tes CMOS Analog Circuit Design - Philip E. Allen and Douglas R. H Press, International Third Edition/Indian Edition, 2013. R. Jacob Baker, Harry W. Li, David E. Boyce, —CMOS Circuit I	Periods ther Open-Lo nparators. Fotal Periods Holberg, Oxfor Design, Layou	9 op Comparators, 45 rd University tt and Simulation ,
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Unit - Characte Improvin Reference 1. 2.	-V COMPARATORS rization of Comparator, Two-Stage, Open-Loop Comparators, O ag the Performance of Open-Loop Comparators, Discrete-Time Com 7 es CMOS Analog Circuit Design - Philip E. Allen and Douglas R. H Press, International Third Edition/Indian Edition, 2013. R. Jacob Baker, Harry W. Li, David E. Boyce, —CMOS Circuit J IEEE Press Series on Microelectronics Systems Stuart K. Tewksh Debaprasad Das, —VLSI Design, Oxford University Press, 2 nd ed ces	Periods ther Open-Lo nparators. Fotal Periods Holberg, Oxfor Design, Layou Duy, Series Ed	9 op Comparators, 45 rd University tt and Simulation I,
Unit - Characte Improvin Reference 1. 2. 3.	V COMPARATORS rization of Comparator, Two-Stage, Open-Loop Comparators, O ng the Performance of Open-Loop Comparators, Discrete-Time Comparators, Disc	Periods ther Open-Lo nparators. Fotal Periods Holberg, Oxfor Design, Layou Duy, Series Ed lition ,2015	9 op Comparators, 45 rd University at and Simulation, ition,1998.

Former Signature of BOS Chairman ECE

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a			-		knowled	-				-			K2				
Course	_				knowled							•	-	K2	2		
Outcom	e		CO3: Apply convolution and IIR Filters concept in signal processing applications.											K3	3		
			CO4:Design Bit level and redundant arithmetic Architectures. CO5:Acquire the knowledge of numerical strength reduction.												5		
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Pre-requ	uisites	Digi	ital Sigr	nal Proc	essing												
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	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO	8 PO	9 P(10		PO 12	PSO 1 3	PSO 2 2	PSO 3		
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Unit – I	INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS	Periods	9
	o DSP Systems -Typical DSP algorithms; Iteration Bound – o	• •	^
^	d iteration bound, Longest path Matrix algorithm; Pipelining	• •	e
Pipelining of I	FIR digital filters, parallel processing, pipelining and parallel	processing for	low power.
Unit – II	REDUCTION	Periods	9
-	finitions and properties; Unfolding - an algorithm for Unf		
	reduction and parallel processing application; Algorithmic	-	
transforms – 2	2-parallel FIR filter, 2-parallel fast FIR filter, DCT algorithm a	rchitecture tra	nsformation,
parallel archite	ectures for rank-order filters, Odd- Even Merge- Sort architec	ture, parallel ra	ank-order filters.
Unit – III	FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS	Periods	9
Fast convoluti	on - Cook-Toom algorithm, modified Cook-Toom algorithm,	Pipelined and	parallel recursive
filters - Loc	k-Ahead pipelining in first-order IIR filters, Look-Ahea	d pipelining	with power-of-2
decomposition	n, Clustered look-ahead pipelining, Parallel processing of IIR	filters, combin	ed pipelining and
parallel proces	ssing of IIR filters.		
Unit – IV	SCALING, ROUND-OFF NOISE, BIT-LEVEL ARITHMETIC ARCHITECTURES	Periods	9
Scaling and re	ound-off noise – scaling operation, round-off noise, state varia	ble description	n of digital filters,
Design of Lyo	 parallel multipliers with sign extension, parallel carry-rip on's bit-serial multipliers using Horner's rule, bit-serial FIR usingHorner'sruleforprecisionimprovement,DistributedArithm 	filter, CSD rep	presentation, CSD
Unit – V	NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING	Periods	9
Numerical stre	ength reduction – sub expression elimination, multiple constant	nt multiplication	on, iterative
matching, syn	chronous pipelining and clocking styles, clock skew in edge-t	riggered single	phase clocking,
Two-phase clo	ocking, wave pipelining. Asynchronous pipelining bundled da	ta versus dual	rail protocol.
		Fotal Periods	45
References			
	K.Parhi, "VLSI Digital Signal Processing Systems", John-Wil	9 ·	
2. U.		2014	
E-Resources	Meyer -Baese, "Digital Signal Processing with FPGAs", Sprin	igei, 2014	
	Meyer -Baese, "Digital Signal Processing with FPGAs", Sprin		
E1 1			
E1 E2 h	Meyer -Baese, "Digital Signal Processing with FPGAs", Sprin https://dl.amobbs.com/bbs_upload782111/files_18/ourdev_48 https://books.google.co.in/books/about/VLSI_DIGITAL_SIGE S_D.html?id=APFRHFkMqG8C	0582.pdf	SSING_SYSTEM
E1 E2 E2 E2	Meyer -Baese, "Digital Signal Processing with FPGAs", Sprin https://dl.amobbs.com/bbs_upload782111/files_18/ourdev_48 https://books.google.co.in/books/about/VLSI_DIGITAL_SIGN	0582.pdf	SSING_SYSTEM

		EKANANDHA COL Autonomous Institutio Elayampa	n, Affil	iated to	o Anna	Universit	ty ,Chennai)	N SD					
Programme	M.E.		Pro	gramn	ne Code	205	Regulation		2023				
Department		DESIGN / ELECTRO IUNICATION ENG					Semester		Ι				
			Perio	ls Per	Week	Credit	Maximu	m Mar	ks				
Course Code		Course NameLTPCCAESLLLLLLLL											
P23VD103		System ratory-I	0	0	4	2	60	40	100				
Course Objective	The ma	ain objective of the co To design a sequent To implement ALU To simulate circuits To simulate circuits To implement DSP	tial circu and MA using X using N	AC in Kilinx/ /IATL	FPGA EDA T	ool							
Course Outcome	CO1:] CO2: CO3: CO4:	At the end of the course, the student should be able toKnowledge LevelCO1: Design a sequential circuit using HDLK4CO2 : Implement ALU and MAC in FPGAK4CO3 : Analyze Circuit simulation using Xilinx/EDA ToolK3CO4 : Analyze Circuit simulation using MATLAB/EDA ToolK3CO5 : Implement DSP AlgorithmsK2											
Pre-requisites	-	1											

	CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak													CO/PSO Mapping		
Cos													PSOs			
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3	
CO 1	3				3								3	2		
CO 2	3				3								3	2		
CO 3	3				3								3	2		
CO 4	04 3 3													2		
CO 5	3				3								3	2		

Direct

- 1. Pre lab and Post lab Test.
- 2. End-Semester examinations

Indirect

1. Course – end survey

Conter	nt of the syllabus	
S.No	Suggested List of Experiments:	CO Mapping
1	Modeling of Sequential Digital system using VHDL	CO1
2	Modeling of Sequential Digital system using VERILOG	CO1
3	Design and Implementation of ALU using FPGA	CO2
4	Simulation of NMOS and CMOS circuits using Xilinx/EDA Tool	CO3
5	Modeling of MOSFET using C	CO4
6	Implementation of FFT, Digital Filters in DSP Processor	CO4
7	Implementation of DSP algorithms using software package	CO5
8	Implementation of MAC Unit using FPGA	CO2
	Total Periods	45
Refere	nces	
1.	An Introduction to VHDL overview, Dinesh Sharma, 2008. vhdl-overview.pdf (iitb.a	uc.in)
2.	U. Meyer -Baese, —Digital Signal Processing with FPGAsl, Springer, 2014	
E-Reso	burces	
E1	Synthesis of Digital Systems - Course (nptel.ac.in)	
E2	Matlab Programming for Numerical Computation - Course (nptel.ac.in)	

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		EKANAND Iomous Inst Elay		WOM filiated	I <mark>EN</mark> to Ann	a Univ	ersity ,C		ISO 001/2015					
Programme	M.E.	Programm	ne Code				205	Regul ation	202	3				
Department		DESIGN/ 1 MUNICAT					Seme	ster	I	Ι				
Course Code		Course Nar	ne	Perio L	ds Per T	Week P	Credit C	CA	Maximum Ma ESE	rks Total				
P23VD104		ronic Desig nation lab	n	0	0	4	2	60	40	100				
Course Objective	•	To introdu	e understar e exposure ce backgro	nding of to diffe ound in	erent H assessi	DL mo	deling st impact o	yles and	their application	esis.				
a	CO1 :	end of the contract of the con	l various r	nodelin	g styles	5.				2				
Course Outcome		Apply mod Verify and s.								<u>.3</u> .4				
		Evaluate the Develop R'						ns.		15 12				
Pre-requisites														
(3/2/	/1 indicate	es strength of		n) 3-Stro	ng, 2 –		n, 1 - Wea	k	CO/PSO Mapping					
PO 1	PO 2 P	03 PO4	Programme Outcomes (POs) PSOs											

Cos]	Program	nme Out	comes (POs)					PSOs		
	PO 1	1 PO 2 PO 3 PO 4 PO 5 PO 6 PO 7 PO 8 PO 9 PO 10 11												PSO 2	PSO 3
CO 1	3	2	2										3	2	
CO 2	3	2	3										3	2	
CO 3	3	2	2										3	2	
CO 4	3	3 2 3												2	
CO 5	3	2	2										3	2	

Direct

- 1. Pre lab and Post lab Test.
- 2. End-Semester examinations

Indirect

1. Course - end survey

Content of the syllabus

S.No Suggested List of Experiments:

CO Mapping

1	Introduction to HDL Simulation Flow	CO1
2	Structural, Behavioral and Dataflow Modeling in Verilog	CO1
3	Arithmetic Units: Adders and Subtractors	CO2
4	Behavioral Modeling and Verification of Flip-Flops, Registers and Counters	CO3
5	Behavioral Modeling, Synthesis and FPGA implementation of Flip-flops, Registers and Counters	CO3
6	Behavioral Modeling and Verification of Finite State Machines	CO3
7	Dataflow Modeling and Verification of Multiplexers and Demultiplexers	CO3
8	Memory Subsystem Design	CO4
9	Transistor Level implementation of CMOS circuits- Basic Logic Gates: Inverter, NAND and NOR.	CO4
10	Transistor Level implementation of 4:1 Multiplexer	CO4
11	Mini project: Development of HDL code for MAC unit and realization of FIR Filter	CO5
	Total Periods	45
Refere	nces	
1.	Stephen Brown and Zvonko Vranesic, Fundamentals of Digital Logic with Edition, McGraw Hill, 2014.	Verilog Design, Third
2.	Morris Mano and Michael D. Ciletti, Digital Design: With an Introduction Fifth Edition, Pearson Higher Education, 2013.	to the Verilog HDL,
E-Reso	urces	
E1	https://docs.google.com/file/d/0B2om2B98SOeiLTY5WWNaSjh4bm8/edi PFVIEteUUiXDSv8msJOGKg	t?resourcekey=0-

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		KANANDHA COLL utonomous Institution Elayampal	Anna U	(,Chennai)	EN	TÜVRheinland CERTIFIED	80 9001:2015							
Programme	M.E.	Programme Code				205	Regulat	tion	2	023				
Department		DESIGN / ELECTR MUNICATION ENG)		Semester			II				
Course Code		Course Name Periods Per Week Credit Maximum Marks												
Course Code		Course Maine	L	Т	Р	С	CA		ESE	Total				
P23VD205	Low I	Power VLSI Design	3	0	0	3	40		60	100				
Course Objective	•	ain objective of the co To identify sources To identify the pow CMOS To explore the conc To understand the la To study the softwa	of powe er optin ept of p ayout de re desig	nizatio ower o esign a gn for l	n techn optimiza nd spec ow pow	iques bas ation and cial techn ver techn	ed on different estimation a iques.	ent le	evel of m	ethods in				
		nd of the course, the st nalyze different sourc d					factors	Kno	wledge I K4					
Course Outcome	adders	nderstand the differen and multipliers		•		•			K3					
Outcome	reducin	entify and analyze the g power consumption	in adde	ers and	multip	liers	in		K3					
									K2					
	CO5: S circuits	D5: Study different power optimization techniques in design of K4												
Pre-requisites	-													

	CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak												CO/PSO Mapping			
Cos													PSOs	PSOs		
	PO 1	PO1 PO2 PO3 PO4 PO5 PO6 PO7 PO8 PO9 PO PO PO 10 11 12												PSO 2	PSO 3	
CO 1	3	3	2	2								1	3	2		
CO 2	3	3	2	2								1	3	2		
CO 3	3	3	2	2								1	3	2		
CO 4	3 3 2 2 1 1													2		
CO 5	3	2	2	2								1	3	2		

Direct

- 1. Continuous Assessment Test I, II & III
- 2. Assignment, Seminar and Quiz
- 3. End-Semester examinations

Indirect

1. Course – end survey

Content of the syllabus

Unit -	- I	POWER DISSIPATION IN CMOS	Periods	9
Hierarchy	of lim	its of power – Sources of power consumption – Physics of p	power dissipation in	CMOS FET
devices- I	Basic p	rinciple of low power design.		
Unit –	- II	POWER OPTIMIZATION	Periods	9
		ower optimization - Circuit level low power design -		
	ure Le	vel Low Power Design - VLSI Subsystem Design of Add	ders, Multipliers, PL	L, Low Power
Design	TTT	DEGION OF LOW DOWED OMOG	D 1	0
Unit –	111	DESIGN OF LOW POWER CMOS CIRCUITS	Periods	9
Computer	r Arith	metic techniques for low power systems – Reducing Pow	ver Consumption in	Combinational
		al Logic, Memories - Low Power Clock - Advanced		al Techniques,
		iques - Physical Design, Floor Planning, Placement and Ro		
Unit –		POWER ESTIMATION	Periods	9
		ion Techniques, Circuit Level, Gate Level, Architecture		Level, – Logic
Power E	stimati	on – Simulation Power Analysis – Probabilistic Power Anal	ys1s	
Unit -	- V	SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER	Periods	9
		ow Power - Behavioral Level Transform -Algorithms for	Low Power - Softw	are Design for
Low Pow	er.		I	
			Total Periods	45
Reference				
1.		oy& S.C. Prasad, "Low Power CMOS VLSI Circuit Design		
2.		itriosSoudris, ChirstianPignet, Costas Goutis, "Designing C er",Kluwer Academic Publishers, 2002.	MOS Circuits for Lo)W
3.		Kuo and J.H Lou, "Low Voltage CMOS VLSI Circuits", W	viley 1999.	
4		Chandrakasan and R.W. Broadersen, "Low Power Digital C		ver
4.		demic Publishers ,1995.	C ,	
5.	Gar	y Yeap, "Practical Low Power Digital VLSI Design", Kluw	er, 1998.	
6.	Aca	ellatifBellaouar, Mohamed.I. Elmasry, "Low Power Digital demic Publishers, 1995.	C	
7.		es B. Kuo, Shin – chia Lin, "Low Voltage SOI CMOS VLS ey & sons, Inc 2001.	I Devices and Circui	ts",John
E-Resourc	es			
E1	<u>C?</u>	ps://www.google.co.in/books/edition/Low Power Cmos V hl=en&gbpv=1&dq=low+power+vlsi+design&printsec=fro	<u>ntcover</u>	-
E2	htt =ei	ps://www.google.co.in/books/edition/Low_Power_Digital_ n&gbpv=1&dq=low+power+vlsi+design&printsec=frontcov	VLSI_Design/0IfkBv ver	-
E3	htt	ps://www.google.co.in/books/edition/Low_Power_Design_1 n&gbpv=1&dq=low+power+vlsi+design&printsec=frontco	Methodologies/9IzuE	3wAAQBAJ?h

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		EKANANDHA CO pnomous Institution, A Elayampalay	WO Affiliate	MEN d to A	nna Un	iversity,		TÜVRheinland CERTIFIED	ISO 9001:2015			
Programme	M.E.	Program	nme Co	le		205	Regulatio n		2023			
Department		DESIGN / ELECTR MUNICATION EN(1		Semester		II			
Course Code	(Course Name		ls Per		Credit		kimum M				
P23VD206	Testing Verifica Circuita	LTPCCAESETotalag and cation of VLSI30034060100										
Course Objective	The ma	in objective of the co To study the fault m To understand the te To explore the desig To study the fault di To study the Timing	odeling est gene gn for te iagnosis	ration stabili	for con	nbination self test n	al and seque nethods.	ential logi	c circuits.			
Course Outcome	CO1:In: CO2:An CO3:Es CO4: U	 To study the Timing verification of VLSI Circuits the end of the course, the student should be able to Market elementary testing hardware into the VLSI chip K2 Analyze VLSI circuit timing using Logical Effort analysis K4 Estimate and compute the power consumption of a VLSI chip K3 Understand the concept of test generation and simulation. 										
Pre-requisites	-	esign and Verify the		ii cuito.					K3			

	CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak												CO/PSO Mapping			
Cos		Programme Outcomes (POs)											PSOs			
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3	
CO 1	3	3	2	2									3	2		
CO 2	3	3	2	2									3	2		
CO 3	3	3	2	2									3	2		
CO 4	3	3	2	2									3	2		
CO 5	3	3	2	2									3	2		

Direct

- 1. Continuous Assessment Test I, II & III
- 2. Assignment, Seminar and Quiz
- 3. End-Semester examinations

Indirect

1. Course – end survey

Content of	the sy	llabus										
Unit		FUNDAMENTALS OF TESTING	Periods	9								
-		and verification in VLSI design process. Issues in test and v	verification of com	plex chips,								
embedded	d cores	and SOCs; Fundamentals of VLSI testing.										
Unit -	– II	TEST GENERATION AND SIMLUATION	Periods	9								
Automati	c test p	attern generation. Design for testability. Scan design. Test in	nterface and bound	lary scan.								
System te	esting a	nd test for SOCs. Iddq testing.										
Unit -	- III	FAULT MODELS	Periods	9								
Fault mod	lels: D	elay fault testing. BIST for testing of logic and memories. T	est automation.									
Unit -	- IV	DESIGN AND VERIFICATION OF VLSI	Periods	9								
		CIRCUITS										
Design ve	erificat	ion techniques based on simulation, Analytical and Formal a	pproaches. Functi	onal								
verificatio	on of V	LSI circuits.										
Unit	Unit - VTIMING VERIFICATION OF VLSIPeriods9											
		CIRCUITS										
Timing ve	erificat	ion. Formal verification. Basics of equivalence checking and	d model checking.	Hardware								
emulation	1.											
		Te	otal Periods	45								
Reference	S											
1.	M. 1	Bushnell and V. D. Agrawal, "Essentials of Electronic Testin	ng for Digital", Me	emory and								
1.		ed-Signal VLSI Circuits", Kluwer Academic Publishers, 20										
2.		Abramovici, M. A. Breuer and A. D. Friedman, "Digital Sys	tems Testing and	Festable								
3.		ign", IEEE Press, 1990. ropf, "Introduction to Formal Hardware Verification", Sprin	ar Varlag 2000									
3.			<u> </u>									
4.		ashinkar, Paterson and L. Singh, "System-on-a-Chip Verific hniques", Kluwer Academic Publishers, 2001.	cation-Methodolog	yand								
E-Resourc		iniques , Kiuwer Academie i ubrishers, 2001.										
12-ACSUULU		s://www.google.co.in/books/edition/Essentials_of_Electroni	c Testing for Di	γ/ITrtBwA Λ								
E1		AJ?hl=en&gbpv=1&dq=testing+and+verification+in+vlsi&										
		s://www.google.co.in/books/edition/System_on_a_Chip_Ve										
E2	=en	&gbpv=1&dq=P.+Rashinkar,+Paterson+and+L.+Singh,+Sy										
	Met	hodologyand++Techniques&printsec=frontcover										

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				nomous	Instituti	ion, A	ffiliated	l to A	nna U	RING F niversity 637 205	,Chei		EN	TÜVRheinland CERTIFIED	201:2015			
Pro	gramme	M.F	E.				Progra	amme	Code	205	Reg	ulation	n	202	23			
Dep	artment				ELECT						Semester			II				
Course	e Code		Cou	ırse Na	ime	F	Periods			Credit				aximum Marks				
		X/T					L 3	T 0	P 0	$\frac{C}{3}$	($\frac{CA}{40}$	ES		Total 100			
P23VI	D207			[•] Wirel nication			3	0	0	3		40	0	50	100			
					ve of the	cours	se is											
		The						ireles	s com	municati	on							
Course		 To understand the concepts of transceiver architectures. To introduce to the students the low power design techniques 												SI circ	nite			
Objecti	ve								-	of various		-			uns.			
					commu	•	-		aion (5 VLO	i cheu	101					
							•		sizer									
		Δt th	• To learn the VLSI Design of synthesizers. At the end of the course, the student should be able to												Level			
			CO1: Understand the application of VLSI circuits in wireless															
			nunica		and upph	- unon	JI TLA		areo 111					K2				
Course					of vario	ous arc	hitectu	res us	ed in i	mpleme	nting		K3					
Outcom	ne		CO2: Knowledge of various architectures used in implementing wireless systems.															
					imulatio	n of lo	w powe	er tech	niques	s using so	oftware	e		K4				
										U				K2				
	CO4: Learn the VLSI design of wireless circuits. CO5:Learnthe VLSI Design of synthesizers													K2				
Pre-req	uisites	Wire	Wireless Communication															
					CO/PO) Mapi	oing						CO/I	PSO				
	(3/2/	1 indica	ates str					2 - Me	edium,	1 - Weak	C C		Мар					
Cos					Program	me Out	tcomes ((POs)					PSOs	5				
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO	-	РО	РО	PSO	PSO	PSO			
CO 1	2	2	2	2					_	10	11	12	1 3	2	3			
001	3		3	22	+				2	2			3		+			
CO 2	5		3	2	+ +				2				3	2	+			
CO 2 CO 3	3	5		2									3	2				
	3	3											-	2				
CO 3	3 3 3		3	2														
CO 3 CO 4 CO 5	3	3	3															
CO 3 CO 4 CO 5 Course	3 3	3	3															
CO 3 CO 4 CO 5	3 3 Assessm	3 ent Me	3 ethods	2	t I, II &	III				·								
CO 3 CO 4 CO 5 Course	3 3 Assessm Continu	3 ent Me	3 ethods	2 ent Tes	t I, II & I	III												
CO 3 CO 4 CO 5 Course 2 Direct 1.	3 3 Assessm Continu	3 ent Me lous As ment, S	3 thods ssessm emina	2 ent Tes r and Q	uiz	III												
CO 3 CO 4 CO 5 Course 2 Direct 1. 2.	3 3 Assessm Continu Assigni End-Se	3 ent Me lous As ment, S	3 thods ssessm emina	2 ent Tes r and Q	uiz	III												
CO 3 CO 4 CO 5 Course 2 Direct 1. 2. 3.	3 3 Assessm Continu Assigni End-Se	3 ent Me lous As ment, S mester	3 thods ssessm eminar examin	2 ent Tes r and Q	uiz	111												
CO 3 CO 4 CO 5 Course 2 Direct 1. 2. 3. Indirect	3 3 Assessm Continu Assign End-Se ct	3 ent Me lous As ment, S mester	3 thods ssessm eminar examin	2 ent Tes r and Q	uiz	III												
CO 3 CO 4 CO 5 Course 2 Direct 1. 2. 3. Indirect 1.	3 3 Assessm Continu Assign End-Se ct	3 ent Me lous As ment, S mester - end s	3 sthods ssessm eminate examinate urvey	2 ent Tes r and Q	uiz	III												
CO 3 CO 4 CO 5 Course 2 Direct 1. 2. 3. Indirect 1.	3 3 Assessm Continu Assign End-Se ct Course	3 ent Me lous As ment, S mester - end s	3 ssessm eminal exami urvey	2 ent Tes r and Q nations	uiz			ΓΙΟΝ	BAS	ICS	Perio	 //ds						

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modulatio	n schemes- classical channel- wireless channel description- p	ath loss- multipath	fading-basics							
of spread	spectrum and spread spectrum techniques- and Direct sequen	ce	-							
Unit – I	TRANSCEIVER ARCHITECTURE	Periods	9							
Transceiv	er design constraints- baseband subsystem design- RF subsys	tem design- Super	heterodyne							
receiver a	nd direct conversion receiver- Receiver front-end- filter desig	n- non-idealities a	nd design							
parameter	s- derivation of noise figure and IP3 of receiver front end.									
	Unit – III LOW POWER DESIGN TECHNIQUES Periods									
	urce of power dissipation- estimation of power dissipation- reducing power dissipation at device and									
	ls- low voltage and low power operation- reducing power dis	sipation at archited	cture and							
algorithm l										
Unit – IV		Periods	9							
	sign of LNA-wideband and narrow band-impedance mat									
	nplifier-power amplifier- Active mixer- analysis, conversion									
	and high frequency case, noise. Passive mixer- sampling mix	xer and switching 1	nixer- analysis							
	on, conversion gain and noise in these mixers.									
Unit – V		Periods	9							
	n of Frequency Synthesizers (FS) – Parameters of FS - PLI	A	•							
•	ctor/charge pump- dividers- VCO- LC oscillators- ring oscilla	tor- phase noise- l	oop filter-							
description	design approaches		1							
		Total Periods	45							
References										
1.	Bosco Leung, "VLSI for Wireless Communication", Spring									
2.	Elmad N Farag and Mohamed I Elmasry, "Mixed Signal VI	SI Wireless Desig	n-Circuits and							
۷.	Systems", Kluwer Academic Publishers, 2002.									
E-Resources	3									
		V · IIT DEI HI								
E1	https://nptel.ac.in/courses/117102062/CO-ORDINATED B									

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		EKANANDHA CO omous Institution, Elayampalay	y ,Chennai)	TÜVFriedrand CENTIFED 0 1995/0915							
Programme	M.E.		2	2023							
Department		DESIGN / ELECTI MUNICATION EN		II							
Course Code		Course Name	Period	ls Per	Week	Credit	Max	ximum Ma	irks		
Course Coue				Т	Р	С	CA	ESE	Total		
P23VD208	VLSI Labor	0	0	4	2	60	40	100			
Course Objective	•	ain objective of the co To know and unders To understand the do To analyze the powe Obtain the layout of To study this course MOS circuits.	tand HD esign of er and tin digital d	various ning of esign	ng EDA tools volved in the designof						
Course Outcome									Knowledge Level K3 K3 K3 K4 K4 K4		
Pre-requisites	-										

	(3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak												CO/PSO Mapping			
Cos		Programme Outcomes (POs)										PSOs				
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3	
CO 1	3				3								3	2		
CO 2	3				3								3	2		
CO 3	3				3								3	2		
CO 4	3				3								3	2		
CO 5	3				3								3	2		

Course	Assessment Methods	
Direct		
1.	Pre lab and Post lab Test.	
2.	End-Semester examinations	
Indired	et	
1.	Course - end survey	
Content	of the syllabus	
S.No	Suggested List of Experiments	CO Mapping
		20
		30

Flum Signature of BOS Chairman ECE 30

	HDL SIMULATION AND IMPLEMENTATION OF FPGA:							
1	Design and Implementation of 8 Bit ALU in FPGA / CPLD	CO1						
2	Design and Implementation of Elevator controller using embedded microcontroller	CO2						
3	Design and Implementation of Alarm clock controller using embedded microcontroller	CO2						
4	Design and Implementation of model train controller using embedded microcontroller	CO2						
5	Design and Simulation of FIR filter using HDL	CO1						
	BACK-END EDA TOOL EXPERIMENTS:							
6	Design and simulation of Multiplier using EDA Tools	CO3						
7	Design and simulation of SRAM using EDA Tools CO3							
8	Design and simulation of Adders using Tanner EDA Tools	CO4						
9	Mini project in CMOS digital circuits	CO5						
	Total Periods	45						
Referen								
1.	BehzadRazavi, "Design of Analog CMOS Integrated Circuits", Edition 2002, M reprint 2017.	cGrawHill Edition						
2.	David A. Johns, Martin K, "Analog Integrated Circuit Design", John Wiley& So 2013.	ons, Inc., New York,						
E-Reso	irces							
E1	ESim - EDA tool for circuit design, simulation, analysis and PCB design - Course	se (swayam2.ac.in)						
E2	Digital Electronic Circuits - Course (nptel.ac.in)							

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	VIVE (Auton		i)	CENT/FED UV:Rutated CENT/FED U 7500e15											
Programme	M.E.]	Progra	mm	e Code	205	Regulatio	on	2023			
Department	VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERINGSemester]	I		
Course Code	(Cours	e Nam		Pe	riods I	Per	Week	Credit	N	laximu	m Mar	ks		
Course Coue		Course		le	L	,	Г	Р	C	CA	E	SE	Total		
P23VD209	VLSI Design Verification and Testing004260Laboratory004260										40	100			
Course Objective	•	 To implement and verify Finite State Machines using Verilog File I/O To study different types of TBs. To analyze the Verification Planning for FIFO/UART To write assertions for FIFO. 													
	At the en			,					0		Knov	Knowledge Level K3			
Course Outcome	CO2: In I/O Dest		nent ar	nd verify	Finite	e State	Ma	chines	using V	erilog File		K	2		
	CO3:Ur	nderst	and di	fferent t	ypes o	of TBs	•					K	2		
	CO4: V	'erify	Planni	ing for F	IFO/L	JART.						K.	3		
	CO5: W	Vrite a	ssertio	ns for Fl	FO.							K	2		
Pre-requisites	-														
	2/1 indicate	es stre		CO / PO			2 -	Mediu	m. 1 - W	eak		/PSO pping			
(3/2				or i or ut		- i o i i g,		1.100101	,	~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~	1.166	PSOs			
(3/2 Cos			0	Programi	ne Out	comes	(PO	s)							

Cos		Programme Outcomes (POs)												PSOs			
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3		
CO 1	3	2	2	2	3				2				3	2			
CO 2	3	2	2	2	3				2				3	2			
CO 3	3	2	2	2	3				2				3	2			
CO 4	3	2	2	2	3				2				2	2			
CO 5	3	2	2	2	3				2				2	2			

Course	Assessment Methods	
Direct		
1.	Pre lab and Post lab Test.	
2.	End-Semester examinations	
Indire	ct	
1.	Course - end survey	
Conten	t of the syllabus	
S.No	Suggested List of Experiments	

CO Mapping

1	Verilog Simulation and RTL Verification a) Memory b) Clock Divider and Address Counter n-Bit Binary Counter and RTL Verification	CO1
2	Finite State Machines Implement and Verify Using Verilog File I/O.	CO2
3	Different types of TBs for memory and adder/subtractor.	CO3
4	Basic Verification environment for FIFO/UART.	CO2
5	Verification Planning for FIFO/UART a) Development of the test cases as per the verification plan b) Generation and Analysis of Code coverage Reports.	CO1
6	Writing assertions for FIFO.	CO5
7	Design and Verification of Ripple Carry Adder (Dataflow, Structural, Gate level, Behavioral, Test bench creation).	CO2
8	Gate level analysis of different stuck at faults in a CMOS Gate (NAND, NOR).	CO1
9	Design of a LFSR and calculate the different power dissipation for the circuit (8bit, 16bit, 32 bit) using BIST.	CO2
10	Perform timing analysis for a given sequential circuit.	CO4
	Total Periods	s 45
Refer	Total Periods	s 45
Refer	Total Periods ences M. Buchnell and V. D. Agravel. "Escentials of Electronic Testing for Digital	
	Total Periods ences M. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing for Digital Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2000.	", Memory and
1	Total Periods Total Periods ences M. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing for Digital Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2000. M. Abramovici, M. A. Breuer and A. D. Friedman, "Digital Systems Testing Design", IEEE Press, 1990.	", Memory and and Testable
1	Total Periods Total Periods ences M. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing for Digital Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2000. M. Abramovici, M. A. Breuer and A. D. Friedman, "Digital Systems Testing Design", IEEE Press, 1990. T.Kropf, "Introduction to Formal Hardware Verification", Springer Verlag, 2 P. Pashinkar, Paterson and L. Singh, "System on a Chin Varification Method	", Memory and and Testable 000.
1 2 3 4	Total Periods Total Periods ences M. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing for Digital Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2000. M. Abramovici, M. A. Breuer and A. D. Friedman, "Digital Systems Testing Design", IEEE Press, 1990. T.Kropf, "Introduction to Formal Hardware Verification", Springer Verlag, 2 P. Rashinkar, Paterson and L. Singh, "System-on-a-Chip Verification-Method	", Memory and and Testable 000.
1 2 3 4	Total Periods Total Periods ences M. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing for Digital Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2000. M. Abramovici, M. A. Breuer and A. D. Friedman, "Digital Systems Testing Design", IEEE Press, 1990. T.Kropf, "Introduction to Formal Hardware Verification", Springer Verlag, 2 P. Rashinkar, Paterson and L. Singh, "System-on-a-Chip Verification-Method Techniques", Kluwer Academic Publishers, 2001. ources https://nptel.ac.in/courses/106103116/Prof.SanthoshBiswas	", Memory and and Testable 000. dology and
1 2 3 4 E-Res	Total Periods Total Periods ences M. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing for Digital Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2000. M. Abramovici, M. A. Breuer and A. D. Friedman, "Digital Systems Testing Design", IEEE Press, 1990. T.Kropf, "Introduction to Formal Hardware Verification", Springer Verlag, 2 P. Rashinkar, Paterson and L. Singh, "System-on-a-Chip Verification-Method Techniques", Kluwer Academic Publishers, 2001. ources https://nptel.ac.in/courses/106103116/Prof.SanthoshBiswas https://www.elprocus.com/ripple-carry.adder-working-types-and.its-application	", Memory and and Testable 000. dology and

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DESIGN / El IUNICATIO Course Name Course	of the control of the control of the control of the number of the number of the interface.	Prog DNICS A INEERI Periods L 3 urse is ew of Em nemory con cing Con	ramme ND NG Per W T 0	Code /eek P 0 d Syste	205 Credit C 3	Reg Se	CA	imum ES	202 I Mark SE 50	[
AUNICATIC Course Name added System n ain objective To study th To learn al To study th To know a To study a	of the control of the control of the control of the number of the number of the interface.	Periods L 3 urse is ew of Em nemory c cing Con	NG Per W T 0 bedde	P 0 d Syste	C 3	40	Maxi CA	imum ES	Mark E	as Total					
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n ain objective To study tl To learn al To study tl To know a To study a	of the con he overvie bout the n he interfac bout debu	urse is ew of En nemory o cing Con	ıbedde	d Syste				6	50	100					
To study th To learn al To study th To know a To study a	he overvie bout the n he interfac bout debu	ew of Em nemory o cing Con		-	m Desig	m lifa									
			ol.	 The main objective of the course is To study the overview of Embedded System Design life cycle To learn about the memory organization. To study the interfacing Concepts. To know about debugging tool. 											
CO1: Realize the design flow of Embedded systemsCO2:Analyze partition decision and interrupt service routine										Knowledge Level K2 K4					
hardware										K3					
CO4: Analyze various in- circuit tool sets for debugging embedded hardware and memories										K3					
CO5: Apply different testing methods involved in test phase for the design of embedded system										K3					
Co s strength of co	orrelation)	3-Strong		edium, 1	- Weak			Марр							
	-			PO	PO	PO			PSO	PSO					
	105 10	0 107	100	10,	10	11	12	1	2	3					
			_												
					2	$\left \right $									
	<u> </u>		+												
2					2				2	+					
	Utilize basic t are Analyze varic are and memo Apply different of embedded ded systems consistent of c pro- D 3 PO 4 1 2 2 2 2 2 2	Utilize basic tool set us are Analyze various in- circate and memories Apply different testing of embedded system ded systems CO / PO Ma Strength of correlation) Programme O 03 PO 4 PO 5 PO 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	Utilize basic tool set used for de are Analyze various in- circuit tool are and memories Apply different testing methods of embedded system ded systems CO / PO Mapping es strength of correlation) 3-Strong Programme Outcomes O 3 PO 4 PO 5 PO 6 PO 7 2 2 2 2 2 2 2 2 2 2 2	Utilize basic tool set used for debuggin are Analyze various in- circuit tool sets for are and memories Apply different testing methods involv of embedded system ded systems CO / PO Mapping es strength of correlation) 3-Strong, 2 – Me Programme Outcomes (POs) O3 PO 4 PO 5 PO 6 PO 7 PO 8 2	Utilize basic tool set used for debugging software Analyze various in- circuit tool sets for debug Analyze various in- circuit tool sets for debug Apply different testing methods involved in te Apply different testing methods involved in te Of embedded system ded systems CO / PO Mapping es strength of correlation) 3-Strong, 2 – Medium, 1 Programme Outcomes (POs) O 3 PO 4 PO 5 PO 6 PO 7 PO 8 PO 9 2	Utilize basic tool set used for debugging software and are Analyze various in- circuit tool sets for debugging emare and memories Apply different testing methods involved in test phase of embedded system ded system ded system ded system ded system O / PO Mapping es strength of correlation) 3-Strong, 2 – Medium, 1 - Weak Programme Outcomes (POs) O 3 PO 4 PO 5 PO 6 PO 7 PO 8 PO 9 PO 10 2 2 2 2 2 2 2 2 2 2	Utilize basic tool set used for debugging software and are Analyze various in- circuit tool sets for debugging embedded are and memories Apply different testing methods involved in test phase for to of embedded system ded system ded system ded systems CO / PO Mapping es strength of correlation) 3-Strong, 2 – Medium, 1 - Weak Programme Outcomes (POs) O 3 PO 4 PO 5 PO 6 PO 7 PO 8 PO 9 PO 10 11 2	Utilize basic tool set used for debugging software and are Analyze various in- circuit tool sets for debugging embedded are and memories Analyze various in- circuit tool sets for debugging embedded are and memories Apply different testing methods involved in test phase for the of embedded system ded systems CO / PO Mapping ded systems Strength of correlation) 3-Strong, 2 – Medium, 1 - Weak Programme Outcomes (POs) O 9 PO 9 PO 10 PO 11 12 2	CO/PO Mapping CO/P Analyze various in- circuit tool sets for debugging embedded are and memories Analyze various in- circuit tool sets for debugging embedded are and memories Apply different testing methods involved in test phase for the of embedded system ded system ded systems CO/P Mapping CO/PO Mapping CO/P Mapping CO/P Mapping CO/P Mapping Strong, 2 – Medium, 1 - Weak Programme Outcomes (POs) PSOs D 3 P0 4 P0 5 P0 6 P0 7 P0 8 P0 9 P0 P0 PSO 2 3	Utilize basic tool set used for debugging software and are K3 Analyze various in- circuit tool sets for debugging embedded are and memories Analyze various in- circuit tool sets for debugging embedded are and memories Apply different testing methods involved in test phase for the of embedded system CO/PO Mapping CO/PSO Mapping ded systems CO/PSO Strong, 2 – Medium, 1 - Weak Mapping Programme Outcomes (POs) O 3 PO 4 PO 5 PO 6 PO 7 PO 8 PO 9 PO PO PSO PSO 2 3 2 3 2 2 3 2 2 3 2 2 3 2 2 3 2 2 3 2 2 3 2 2 3 2 2 3 2 2 3					

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Unit – I	[EMBEDDED DESIGN LIFE CYCLE	Periods	09						
		cation - Hardware / Software partitioning - Detailed ha								
		oduct testing – Selection Processes – Microprocessor Vs N								
		king-RTOSMicroController-Performancetools-Benchmark	ang-RTOSavai	lability – Tool						
chain availa	DIIIT	y – Other issues in selection processes.								
Unit – Il		PARTITIONING DECISION	Periods	09						
		ware duality – coding Hardware – ASIC revolution – Manag								
		nment – memory organization – System startup – Hardwar	e manipulation	- memory						
mapped acco	ess -	- speed and code density.	Γ	Γ						
Unit – II		INTERRUPT SERVICE ROUTINES	Periods	09						
		s – Flash Memory basic toolset – Host based debugging – I ic analyzer – Caches – Computer optimization – Statistical		ng – ROM						
	Ŭ		Ŭ							
Unit – IV		IN CIRCUIT EMULATORS	Periods	09						
		control – Real time trace – Hardware break points – Overla	y memory – Tir	ning constraints						
– Usage issu										
Unit – V	7	TESTING	Periods	09						
		eduction of risks & costs - Performance - Unit testing - Re								
cases – Fund Maintenance		al tests – Coverage tests – Testing embedded software – Pe	rformance testir	ıg —						
Withittenturies	0.	r	Fotal Periods	45						
References										
1. A	Arno	ld S. Berger, "Embedded System Design", CMP books, US.	A 2017.							
2. F	Frank	v Vahid, Tony Givargis, "Embedded System Design-A Unifi	ed Hardware/So	oftware						
4.	Introduction",2018									
3. E	Embe	edded / Real-Time Systems: Concepts, Design and Program	ming, Dr. K.V.H	K Prasad,2013						
E-Resources										
E1 h	ttps:	//nptel.ac.in/courses/106105159/,Prof.anupambasu, IIT Kha	aragpur							
E2 h	ttps:	//www.globalspec.com/reference/28434/203279/chapter-1-	the-embedded-d	esign-life-cycle#						

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C			VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution, Affiliated to Anna University ,Chennai)											TÛV	ISO 9001:2 Rheinland		
			Elayampalayam, Tiruchengode – 637 205											D \$105048155			
Pro	gramme						Ŭ		e Code	e 20	05	Reg	n 2023				
Dep	artmen		VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING Semester									Ι					
Course	e Code		Course Name Periods Per Week Credit Max L T P C CA							aximum Marks ESE Tota							
P23VDE02			Physics of MOS300340Transistors											60	100		
		The	e main	objecti	ve of th	e cours	se is										
			• To provide an in-depth knowledge in VLSI Design methodology.														
Course			• To enhance the fundamentals of different scaling rules.														
Objecti	ve		• T	o study	/ Small	Signal	Analy	sis									
÷				•	V NANO	0	•										
				-	v proper		-										
					ourse, tl					0				Knov	wledge	Level	
Carre		CO	CO1:Analyze a NANO MOS transistor model											K4			
Course Outcon	ne		CO2:Understand Scaling Rules for transistors structures											K2			
Juicon			CO3: Design and analysis of circuits in different scaling.										K3,K6				
			CO4:Analyze small signal transistor									K4					
			CO5:Understand different optical properties									K2					
Pre-req	uisites	EDO	С														
	(2)(/1 '			CO/PO			2 1	(1'	1 5	X 71			CO/			
Cos	(3/2	2/1 111010	indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak Programme Outcomes (POs)								1	Mapping PSOs					
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO			PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3	
CO 1	3	3	2	2								2			3		
CO 2 CO 3	3	3	23	23								2		2	3		
CO 4	3	3	3	2								2		3	5		
CO 5	3	3	3	2										2			
Course	Assessn	nent M	ethods														
Direct																	
1.					t I, II &	III											
2. 3.			Semina r exami														
J. Indire		emeste	i exami	nations													
1.		e - end	survey														
1.																	
	of the c																
Content					MO	TRAI	NSIST	ORS	1				Per	iods		9	
Content	t of the states				MOS	S TRAI	NSIST	ORS	5				Per	riods		9 36	
Content					MOS		<\$	Se					Per	riods		-	
Content					MOS			Se			ECE]	Per	iods		9 36	

effects in	transistor: Pao-Sah and Brews models; Short channel effect MOS transistors; Quasi-static compact models of MOS tran		
Unit -	n, Measurement of MOS transistor parameters. II SCALING RULES	Periods	9
	nd transistors structures for ULSI; Silicon-on-insulator trans	sistors; High-field and rad	liation effects
	ors, The bipolar transistor.		
Unit –		Periods	9
	oll model; charge control model; small-signal and switching		
graded- e	mitter transistors; High-current and high- frequency effects;	Hetero junction bipolar t	ransistors;
Junction	FETs; JFET, MESFET and hetero junction FET.		
Unit –	IV NANO MOS TRANSISTOR	Periods	9
hydrogen limits of	ger equation, states and operators, particle-in-a-box, density atom, tunneling, two-level systems. Electrons in a crystal la MOS operations.	attice, quantum effects, Fu	undamental
Unit -		Periods	9
	s equations in dielectric media, polarization in insulators, fe i indirect transitions in semiconductors, excitons, optoelectr		
Reference	S	ł	
1.	R.M.Warner, B.L.Grung, "MOSFET – Theory and Des University Press, 1999.	sign", Published by Oxfor	·d
2.	Yannis Tsividis, Colin Mc Andrew "Operation and Mode by Oxford University Press, 2011.	-	
3.	Simon M. Sze, Kwe K. Ng, "Physics of Semiconductor I 2006.	-	ord Edition,
4.	P.I.Varghese, T. Pradeep, A.Ashok Reddy, "A Text Bool	k of Nanoscience and	
т.	Nanotechnology" published by McGraw Hill Education	1 st Edition, 2017.	
E-Resourc	es		
E1	https://nptel.ac.in/courses/117102061/24CO-ORDINATI		
E2	https://nptel.ac.in/courses/115102014/CO-ORDINATED	BY : IIT DELHI	

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		VEKANANDHA Co onomous Institution, Elayampala	WC Affiliat	DMEN ted to A	Anna U	niversity	,Chennai)	TÜVRheitend	SD 9001-2015		
Programme	M.E.	•	Pro	gramm	e Code	205	Regulatio	on 2	023		
Department		DESIGN / ELECTR IUNICATION EN()		Semester		I		
Course Code	C	ourse Name	Period	ds Per	Week	Credit	Ma	ximum Mar	ks		
Course Code	C	ourse maine	L	Т	Р	C	CA	ESE	Total		
P23VDE03	Founda CAD	ations of VLSI	3	0	0	3	40	60	100		
Course Objective	 To learn the basics of physical design process such as partitioning and placement. To analyze the different types of floor planning, placement and routing algorithms. To learn the two level logic synthesis and binary decision diagrams. To learn the synthesis in VLSI physical design automation. At the end of the course, the student should be able to Knowledge Level										
	At the end	Knowledge Level									
	CO1: Und analysis		Into meage	e Level							
	unuijoio	derstand the desig	n metr	nodolog	gies of	VLSI	and graph	K			
	~	derstand the desig					U I		4		
Course Outcome	CO2:Ana CO3: Int		ign proc	cess of	VLSI d	esign flov	w process	K	4		
	CO2:Ana CO3: Int routing a	alyze the physical des erpret the concepts of nd floor planning escribe the concepts	ign proc of physic	cess of cal des	VLSI d ign pro	esign flov ocess sucl	w process n as	K	4 4 5		
	CO2:Ana CO3: Int routing a CO4: De automatic	alyze the physical des erpret the concepts of nd floor planning escribe the concepts on derstand the modeling	ign proc of physic of sim	cess of cal des nulation	VLSI d ign pro	esign flov cess sucl LSI phys	w process n as ical design	K K K	4 4 5 3		

	(3/2	/1 indic	cates str		CO / PO		0	2 – Med	ium, 1 -	Weak			CO/I Map		
Cos	Cos Programme Outcomes (POs)											PSOs			
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1	3	3	2	3										2	
CO 2	3	3	2	3								2		2	
CO 3	3	3	2	3						2		2	3	2	
CO 4	3	3	2	2						2			3		
CO 5	3	2	2	2						2			3		

Direct

- 1. Continuous Assessment Test I, II & III
- 2. Assignment, Seminar and Quiz
- 3. End-Semester examinations

Indirect



1. Cour	e – end survey		
Contont of the	and labore		
Content of the	synabus		
Unit – I	VLSI DESIGN METHODOLOGIES	Periods	9
	o VLSI Design methodologies – Review of Data structures an	-	
-	ation tools – Algorithmic Graph Theory and Computational C		able and
	oblems – general purpose methods for combinatorial optimiza		T
Unit – II	DESIGN RULES	Periods	-
•	action – Design rules – problem formulation – algorithms for	• •	ompaction –
^	d partitioning - Circuit representation - Placement algorithms	· •	
Unit – III	FLOOR PLANNING	Periods	-
-	g concepts - shape functions and Floor plan sizing - Types of	local Routing pro	olems – Area
	nnel routing – global routing – algorithms for global routing.		
Unit – IV	SIMULATION	Periods	-
	Gate-level Modeling and simulation – Switch-level modeling		1-
	al Logic Synthesis – Binary Decision Diagrams – Two Level I	Logic Synthesis.	
Unit – V	MODELLING AND SYNTHESIS	Periods	
	nthesis - Hardware models - Internal representation - Alloca	-	nd scheduling –
Simple schee	uling algorithm – Assignment problem – High level transform	ations.	
		Total Periods	45
Text Books			
	I. Gerez, "Algorithms for VLSI Design Automation", John W	•	
^{2.} Pu	A. Sherwani, "Algorithms for VLSI Physical Design Automation blishers, 2002.	ion", Kluwer Acad	emic
Reference Bo	ok:		
	arafzadeh, C.K. Wong, "An Introduction to VLSI Physical De dition 1995	sign", McGraw Hi	ll International
E-Resources			
E1 htt	os://nptel.ac.in/courses/108102042/CO-ORDINATED BY : II	T DELHI	
E2 htt	os://nptel.ac.in/courses/106102062/ CO-ORDINATED BY : II	IT DELHI	

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E. SI DESIGN DMMUNICA Course N DL with Syst odeling. e main object • To und • To stud HDL. • To und • To und • To und • To und • To und • To und • To und	ATION ame tem ive of th erstand t erstand t erstand t course, th are descr	e course he Concepts he Concepts he Concepts he Concepts he concepts he concepts	Progra NICS A NEERI eriods I L 3 e is cepts of cepts of cepts of cepts of cepts of cepts of cepts of cepts of	Imme C ND NG Per We T 0 (f Hardv ements f Timir ming is f Syste	Code eek C P - o <td< th=""><th>205 redit C 3 escript ogram es and</th><th>Sem (40 ion La ming Syster</th><th>CA anguag of VH</th><th>kimum ES 6 ge.</th><th>50</th><th>s Total 100</th></td<>	205 redit C 3 escript ogram es and	Sem (40 ion La ming Syster	CA anguag of VH	kimum ES 6 ge.	50	s Total 100							
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• To und ne end of the D1:Use hardw cuits using da D2: Analyze o	erstand t course, th are descr	he Cono ne stude iption la	cepts of ent shou	f Syste	 ve To understand the Concepts of Timing Issues and System Modeling in HDL. To understand the Concepts timing issues and Processor model in VHDL 													
01:Use hardw cuits using da 02: Analyze o	are descr	iption la																
cuits using da 02: Analyze o				ld be al	ble to				Know	ledge	Level							
02: Analyze o	CO1:Use hardware description language to design and simulate digital circuits using data flow and behavioral modelingCO2: Analyze of logic circuits by using different levels of																	
uching using	VHDL									K3								
03: Write the ng tech bench	Verilog F	Program	for log	ic circu	its and	synthe	sis by			K3								
CO4: Analyze the timing issues and Processor models																		
		ic conce	epts of S	System	Verilog	5				K2								
tal System D	esign																	
cates strength o	of correla	tion) $\overline{3-5}$	Strong, 2		lium, 1 -	- Weak			Map	oing								
	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	11	PO 12	1	2	PSO 3							
3 2											3							
$\frac{3}{3}$ 2	2						2	2	3	$\frac{2}{2}$	3							
3 2								2		2	3							
3 2	2								3	2	3							
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	ructural modeling	, —
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elay, timing modeling, timing modeling, timing assertion, se	etup and hold tin	nes for
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and Routines: Procedural Statements, Tasks, Functions, and Vo		
	Total Periods	45
Samir Palnitkar, "Verilog HDL: A Guide to Digital Design a	nd Synthesis" 2n	d Edition
		a Danion,
	anning the Test h	anah Languaga
	earning the Test o	ench Language
J.Bhasker, —VHDL Synthesis Primer ^{II} , Prentice Hall.1998		
J.Bhasker, —A Verilog Primer ^I , Prentice Hall 2005.		
Michel D Ciletti, —Advanced Digital Design with Verilog H	DLI, Pearson educ	ation, 2010.
Neil Weste and Kamran Eshranghian, -Principles of CMOS	VLSI DesignI, Ad	dison Wesley,
2000.		
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https://nptel.ac.in/courses/117101004/17CO-ORDINATED	BY : IIT BOMBA	Y
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	at and procedural statements, UDP, sub circuit parameters, func xamples V TIMING ISSUES elay, timing modeling, timing modeling, timing assertion, seices, Processor model, RAM model, UART model V SYSTEM VERILOG Built-in Data Types, Fixed-Size Arrays, Dynamic Arrays, Que ef, Creating User-Defined Structures, Enumerated Types, Cons and Routines: Procedural Statements, Tasks, Functions, and Vo Samir Palnitkar, "Verilog HDL: A Guide to Digital Design a Pearson Education New Delhi, 2019 J.Bhasker Prime, —A Verilog HDL rl, Prentice Hall, 2018 Chris Spear, "System Verilog for Verification: A Guide to L Features", 2nd Edition, Springer, 2012 J.Bhasker, —A VHDL Primer Prentice Hall, 1998. J.Bhasker, —A Verilog Primer Prentice Hall 2005. Michel D Ciletti, —Advanced Digital Design with Verilog H Neil Weste and Kamran Eshranghian, —Principles of CMOS 2000. s https://nptel.ac.in/courses/117101004/17CO-ORDINATED I https://nptel.ac.in/courses/117101004/downloads/Lecture%2	VTIMING ISSUESPeriodselay, timing modeling, timing modeling, timing assertion, setup and hold timices, Processor model, RAM model, UART modelPeriodsVSYSTEM VERILOGPeriodsBuilt-in Data Types, Fixed-Size Arrays, Dynamic Arrays, Queues, Creating Newef, Creating User-Defined Structures, Enumerated Types, Constants, Strings. Proand Routines: Procedural Statements, Tasks, Functions, and Void FunctionsTotal PeriodsSamir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", 2nPearson Education New Delhi, 2019J.Bhasker Prime, —A Verilog HDL rl, Prentice Hall, 2018Chris Spear, "System Verilog for Verification: A Guide to Learning the Test bFeatures", 2nd Edition, Springer, 2012J.Bhasker, —A VHDL Primerl, Prentice Hall, 1998.J.Bhasker, —A VHDL Synthesis Primerl, Prentice Hall, 1998.J.Bhasker, —A Verilog Primerl, Prentice Hall 2005.Michel D Ciletti, —Advanced Digital Design with Verilog HDL!, Pearson educNeil Weste and Kamran Eshranghian, —Principles of CMOS VLSI Designl, Ac2000.shttps://nptel.ac.in/courses/117101004/downloads/Lecture%20Notes/D.K.%205

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Programme	M.E.		Pro	gramm	e Code	205	Regulation	2	2023		
Department		DESIGN / ELECTR MUNICATION EN()		Semester		I		
Course Code		Course Name	Perio	ls Per	Week	Credit		imum Ma	rks		
Course Code		eourse rvanie	L	Т	Р	C	CA	ESE	Total		
P23VDE05	Intro	luction to MEMS	3	0	0	3	40	60	100		
Course Objective											
	At the e		Knowledge Level								
Course	proces	achining	ŀ	K2							
Outcome	CO2:	Analyze etching meth s	ods and	the va	rious n	nodels of	micro	ŀ	K4		
	CO3:	Explore various Micro	actuato	r syster	ns.			ŀ	K2		
		Design Mechanical M		ŀ	K3						
	CO5:]	Interpret optical MEMS		ŀ	K2						
Pre-requisites	-										

	CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak														CO/PSO		
	(3/2	/1 indic	cates str	ength of	f correla	tion) 3-	Strong, 2	2 – Med	ium, 1 -	Weak			Mapping				
Cos	Programme Outcomes (POs)													PSOs			
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	РО	PO	PO	PSO	PSO	PSO		
										10	11	12	1	2	3		
CO 1	3	3	3	2			2			3				2			
CO 2	3	3	3	2			2			3				2			
CO 3	3	3	3	2			2						3	2			
CO 4	3	3	3	2			2						3				
CO 5	3	3	2	2			2						3				

Direct

- 1. Continuous Assessment Test I, II & III
- 2. Assignment, Seminar and Quiz
- 3. End-Semester examinations

Indirect

1. Course - end survey

Unit – I	MEMS FUNDAMENTALS	Periods	9
	Background: Resonant gate transistor (RGT), Silicon Pressur		U
	Mechanical Systems. Micro fabrication and Micromachining	: Integrated C	ircuit Processes,
Bulk Micromac			_
Unit – II	ETCHING METHODS & SENSORS	Periods	9
^	ng and Anisotropic Etching, Wafer Bonding, High Aspect-Ra		
	Classification of physical sensors, Integrated, Intelligent, or		·
A	Thermal sensors, Electrical Sensors, Mechanical Sensors, C		
Unit – III	MICRO ACTUATORS	Periods	9
	s: Electromagnetic and Thermal micro actuation, Mechan	•	
	examples, micro valves, micro pumps, Micromotors- Micro	•	•
heads, Micro-1	nirror TV Projector.; Surface Micromachining: One or t	wo sacrificial	layer processes,
Surface micron	nachining requirements.		
Unit – IV	MECHANICAL MEMS	Periods	9
Poly silicon s	urface micromachining, Other compatible materials, Sili-	con Dioxide,	Silicon Nitride,
Piezoelectric n	naterials, Surface Micro machined Systems : Micro moto	ors, Gear trair	s, Mechanisms.;
Application Ar	eas: All-mechanical miniature devices, 3-D electromagnetic	actuators and	
sensors.			
Unit – V	OPTICAL MEMS	Periods	9
RF/Electronics	devices, Optical/Photonic devices, Medical devi	ices e.g. l	ONA-chip, micro-
arrays.; lab/Des	sign:(two groups will work on one of the following design pr	oject as a part	of the
course),Optical	/Photonic device/system, Medical device e.g. DNA-chip, mid	cro-arrays. Op	tical Switches
		Fotal Periods	45
References			·
1. D	ai Ran Hsu, -MEMS & Micro Systems Design and Manufact elhi, 21 st reprint 2014		
2. P.	Rai-Choudhury - MEMS and MOEMS Technology and Appl	lications, SPIE	Press, 2009
1 1			·
3. St	ephen Santuria, - Microsystems Design, Kluwer publishers, S		
	ephen Santuria, - Microsystems Design, Kluwer publishers, S adimMaluf, - An introduction to Micro electro Mechanical Sy	pringer US, 2	005.
4. N		pringer US, 20 /stem Design, 2	005. Artech House,2004
4. N	adimMaluf, - An introduction to Micro electro Mechanical Sy	pringer US, 20 /stem Design, 2	005. Artech House,2004
4.N5.ME-Resources	adimMaluf, - An introduction to Micro electro Mechanical Sy	pringer US, 20 7stem Design, co Raton, 2002	005. Artech House,2004
4.N5.ME-ResourcesE1htE2htsp	adimMaluf, - An introduction to Micro electro Mechanical Sy Tohamed Gad-el-Hak, The MEMS Handbook, CRC press Bac	pringer US, 20 /stem Design, co Raton, 2002 IIT KHARAC nicroelectrom	005. Artech House,2004 2 GPUR

Former Signature of BOS Chairman ECE

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Programme	M.E.		Pro	gramm	e Code	205	Regulation	2	023		
Department		DESIGN / ELECTR MUNICATION EN()		Semester		I		
Course Code		Course Name		ls Per	Week	Credit		imum Ma			
Course Coue	Ì		L	Т	Р	С	CA	ESE	Total		
P23VDE06	Multin Techni	nedia Compression iques	3	0	0	3	40	60	100		
Course Objective	 To explore the special features and representations of different data types. To analyze different compression techniques for text data and audio signals To analyze various compression techniques for image and video signals. 										
	At the en		Knowledge Level								
	CO1:Us	se Compression techn	iques in	n multi	media.			K	2		
Course	CO2: 1 applicat	Know different text co ion.	ompress	sion teo	chnique	es and its		K	3		
Outcome	CO3: L	earn the concept of va	rious au	dio coi	npressi	on metho	ds.	K	4		
	CO4: Id	lentify various image	compres	ssion te	chnique	es.		K	4		
		CO5: Learn the concept of various video compression techniques and its application.									
Pre-requisites	-										

						2.14	•						CO/PSO			
					CO/PO											
	(3/2	2/1 indic	cates str	ength of	f correla	tion) 3-	Strong, 1	2 - Med	lium, 1 -	Weak			Mapping			
Cos	os Programme Outcomes (POs)									PSOs						
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3	
CO 1	3	3	3	2	2					2		2	3			
CO 2	3	3	3	2									3			
CO 3	3	3	3	2									3	2		
CO 4	3	3	3	2									3	2		
CO 5	3	3	3	2										2		

Direct

- 1. Continuous Assessment Test I, II & III
- 2. Assignment, Seminar and Quiz
- 3. End-Semester examinations

Indirect

1. Course - end survey

Unit		INTRODUCTION	Periods	9
		s of Multimedia - Graphics and Image Data Representat		
		Graphics, Video and Digital Audio - Storage requirement		
		mpression - Taxonomy of compression techniques -	-Error free C	Compression-Lossy
	ression.			
Unit	– II	TEXT COMPRESSION	Periods	9
-		echniques – Huffman coding – adaptive Huffman coding – a		ng –
		coding – dictionary techniques –LZ77, LZ78, LZW family		-
Unit -		AUDIO COMPRESSION	Periods	9
		ssion techniques - μ - Law and A- Law companding - Freque		
		ling -Speech coding standard-G.722-Audio coding stan	dard MPEG a	audio, progressive
		idio – Silence compression techniques.	TT	
Unit -		IMAGE COMPRESSION	Periods	9
		sion: Fundamentals-compression standards-JPEG Standard		
		compression -Implementation using filters - EZW, SPIHT of	coders – JPEG2	2000 standards -
		andards- Run length coding.	<u>. </u>	
Unit		VIDEO COMPRESSION	Periods	9
Video	compres	sion techniques and standards – MPEG Video Coding I: MI	PEG - 1 and 2	– MPEG Video
Coding	g II -MP	EG-4 and 7 – Motion estimation and compensation technic	ques – H.261 S	tandard – DVI
techno	ology – D	VI real time compression – Packet Video.		
		*	Fotal Periods	45
Referen	ces			•
1.		d Sayood, "Introduction to Data Compression", Morgan Kau n, 2012	iffman Harcour	t India, Fourth
E-Resou	rces			
E1	www.	ics.uci.edu/~dan/pubs/DataCompression.html		
E2	https:/	//nptel.ac.in/courses/106105082/38CO-ORDINATED BY :	IIT KHARAG	PUR
E3		//nptel.ac.in/downloads/117105083/CO-ORDINATED BY :	IIT KHARAO	SPUR
FURTH	1			
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	IEEE I	Transactions on "Information Theory".		
2		www.arturocampos.com/compression.html		

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Programme	M.E.	Program	nme Co	de		205	Regulatio	on 2	023
Department	VLSI COMI	I							
Course Code	0	Course Name	Perio	ds Per	Week	Credit		imum Mar	ks
Course Coue			L	Т	Р	С	CA	ESE	Total
P23VDE07	Semicon Design	nductor Memory	3	0	0	3	40	60	100
Course Objective	• • • • •	To acquire knowled To study about arch To comprehend the To study the semico To study the advance	itecture semico onducto	and op nducto r memo	peration r memo pry radi	ns of diff ory reliab iation eff	erent semicon pility.		mories.
	At the en	nd of the course, the st	udent sl	nould b	e able t	0		Knowledge	e Level
	CO1: A	nalyze the different ty	ypes of	RAM,	ROM	designs.		K4	1
Course Outcome	CO2: A	nalyze the different R nects.	RAM an	d ROM	I archit	tecture ar	nd	K	1
Outcome	CO3: A	nalyze the semicondu	ictor me	emory	eliabil	ity.		K4	1
	CO4: A	nalyze the radiation e	effects of	of semio	conduc	tor memo	ories.	K?	3
	CO5: Id design.	entify the new develo	opment	s in sen	nicondu	uctor mer	mory	K	3
Pre-requisites	EC-I &	Ι					ł		
		CO / PO M	apping					CO/PSO	

	(3/2	/1 indic	cates str	ength of		tion) $\overline{3}$ -S	Strong, 2	2 – Med	ium, 1 -	Weak			CO/I Map	ping	
Cos]	Program	ime Out	comes (POs)					PSOs	5	
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	РО	PO	РО	PSO	PSO	PSO
										10	11	12	1	2	3
CO 1	3	3	2	2						2			3	2	
CO 2	3	3	2	2						2				2	
CO 3	3	3	2	2						2				2	
CO 4	3	3	2	2							3		3		
CO 5	3	3	2	2							3		3		

Direct

- 1. Continuous Assessment Test I, II & III
- 2. Assignment, Seminar and Quiz
- 3. End-Semester examinations

Indirect

1. Course - end survey

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Content of	the sy	llabus		
Unit – I	I	RANDOM ACCESS MEMORY TECHNOLOGIES	Periods	9
cell and pe Advanced access Me advanced	eriphe SRA emorie cell s	Access Memories (SRAM): SRAM cell structure, MOS SR ral Circuit Operation, Bipolar SRAM Technologies, Silicon M Architectures and Technologies, Application Specifie es (DRAM): DRAM Technology Development, CMOS D tructure, BiCMOS DRAM, soft error failure in DRAM, oplication Specific DRAM	on Insulator (d SRAMs. D RAM, DRAM	SOI) technology. Dynamic Random 1 cell theory and
Unit – I	I	NON- VOLATILE MEMORIES	Periods	9
PROMs, programm	Erasa able re, No	nly Memories (ROM), High density ROMs, Programmable ble (UV) programmable ROM (EPROM), Floating, C EPROM (OTPEPROM), Electrically Erasable PROMS on Volatile SRAM, Flash Memories (EPROM and EEPF	Gate EPROM S, EEPROM	cell, one time Technology and
Unit – I	II	SEMICONDUCTOR MEMORY RELIABILITY	Periods	9
Reliabilit	y mo	ility issue- RAM Failure modes and Mechanism- deling and failure rate prediction- Design for reliability ening and qualification.		nory Reliability- y test structure-
Unit – I		SEMICONDUCTOR MEMORY RADIATION EFFECTS	Periods	9
e		enomenon (SEP). Radiation Hardening Technique- Radiation hardened memory characteristics — Radiation hardness assumed to the second sec	• •	e e
Unit – V		ADVANCED MEMORY TECHNOLOGY	Periods	9
		ndom Access Memories (FRAMs) – Gallium Arsenide (GaA /e RAMs (MRAMs) - Experimental memory device.	As) FRAMs –	Analog Memories
			Total Period	s 45
References		ok K Sharna, "Semiconductor Memories Technology", Test	ing and Reliat	oility. Wiley 2002.
2.	Ash	ok K Sharna, "Advanced Semiconductor Memories–Archi lications", Wiley2002.		
3.	Anj	anGhosh, "High Speed Semiconductor Devices", NPTEL Co	ourseware, 200)9.
E-Resource	s			
E1		p://www.bitsavers.org/pdf/ti/_Texas_Instruments_Electronic Memory_Design_and_Application_1973.pdf	cs_Series/Lueo	cke_Semiconducto
E2	-	s://archive.nptel.ac.in/courses/117/101/117101058/		
E3		s://books.google.co.in/books/about/Semiconductor_Memori dir_esc=y	es.html?id=Vl	NsmAQAAMAAJ

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Course	Code		Cou	rse Na	me	P	eriods L	Per W T	Veek P	Credit C		Max CA	ximum Marks ESE Tota					
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		•]	Го un	derstan	d the c	oncepts	s of SO	C De	sign n	nethodo	logy fo	r Logic	c Core	es.				
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Objectiv	ve			g Cores		r	· ~ j ·			r <i>c</i>		2	, y		-)			
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Outcom	e	memo				e pro o					101		K2					
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CO 2 CO 3	3	$\frac{3}{3}$ $\frac{2}{3}$	-	2					2			2	3	2	+			
CO 4	3	3 2		2				1		2			-	2				
CO 5	3	3 3	3	2						2				2				
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Unit –	I INTRODUCTION	Periods	9
System tra	deoffs and evolution of ASIC Technology- System on ch	ip concepts and method	ology – SOC
design issu	ies -SOC challenges and components.		
Unit – I	II DESIGN METHODOLOGICAL FOR LOO CORES	GIC Periods	9
SOC Desig	gn Flow – On-chip buses –Design process for hard cores	–Soft and firm cores –E	Designing with
hardcores,	soft cores- Core and SOC design examples.		0
Unit – I	II DESIGN METHODOLOGY FOR MEMO AND ANALOG CORES	RY Periods	9
Embedded	memories -Simulation modes Specification of analog cir	rcuits – A to D converte	er – Phase- located
loops –Hig			
Unit – I		Periods	9
	validation - Test benches - SOC design validation - Co st	imulation -hardware/ S	oftware co-
	n. Case Study: Validation and test of systems on chip.		
Unit – '		Periods	9
	Issues – Testing of digital logic cores –Cores with bound		
	ting of microprocessor cores - Built in self method -testi	ing of embedded memor	ries. Case Study:
Integrating	BIST techniques for on-line SOC testing.		
		Total Periods	45
References			
1.	Rochit Rajsunah, "System-on-a-Chip: Design and Test"	", Artech House, 2007.	
2.	Prakash Raslinkar, Peter Paterson & Leena Singh, "Sys	stem-on-a-Chip Verifica	tion: Methodolog
۷.	and Techniques", Kluwer Academic Publishers, 2000.	-	-
3.	M.Keating, D.Flynn, R.Aitken, A, GibbonsShi, "Low P	Power Methodology Ma	nual for System-
5.	on-Chip Design Series: Integrated Circuits and Systems		
	L.Balado, E. Lupon, "Validation and Test of Systems	on Chip", IEEE confere	ence on SIC/SOC
4.	1999.		
	A.Manzone, P.Bernardi, M.Grosso, M. Rebaudenge		
4. 5.	A.Manzone, P.Bernardi, M.Grosso, M. Rebaudenge Ricerche Fiat, "Integrating BIST Techniques for On-lin		
	A.Manzone, P.Bernardi, M.Grosso, M. Rebaudenge		
	A.Manzone, P.Bernardi, M.Grosso, M. Rebaudenge Ricerche Fiat, "Integrating BIST Techniques for On-lin On-Line testing, 2005.		
5.	A.Manzone, P.Bernardi, M.Grosso, M. Rebaudenge Ricerche Fiat, "Integrating BIST Techniques for On-lin On-Line testing, 2005.	ne SoC Testing", IEEE	

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Course	e Code			urse Na		Р	eriods L		Week P	Credit C		Ma CA	ximum ES		as Total			
P23A	C001	Research Process and Methodologies200100The main objective of the course is																
Course Objectiv	ve	The	ToTo	unders acquir	stand the e knowle	impo edge in	rtance n Data				ysis							
		To effectively write reports At the end of the course, the student should be able to CO1: Understand research problem types and data collection											Know	vledge K2	Level			
Course		methods. CO2: Understand research design methodologies												K2				
Outcom	le	CO3: Analyze research related information CO4: Follow research ethics												K4 K2				
		Info	rmatio		that toda nology, l tivity.							eas,	K2					
Pre-req	uisites																	
	(3/2	/1 indic	ates str	ength of	CO / PO f correlati	on) 3-	Strong			1 - Weak			CO/F Map	ping				
Cos	PO 1	PO 2	PO 3	PO 4	Programr	ne Out PO 6	comes	(POs			- BO	DO	PSOs PSO	PSO	DEO			
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CO 2	3	3	3	2					2									
CO 3 CO 4	3	3	3	2				_	2		-							
CO 4 CO 5	3	3	3	2	+				2		+				+			
	-	-		-			1		I		1	1	<u> </u>		1			
Direct																		
1. 2.	Assign				t I, II & I	II												
Indirec																		
1.	Course	- end s	survey															

Content of the syllabus

Unit - I

INTRODUCTION TO RESEARCH 9 Periods Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research Meaning of Research - Types of Research - Research Process - Problem definition - Objectives of Research -Research design - Approaches to Research - Quantitative vs. Qualitative Approach - Research Methods versus Methodology - Research and Scientific Method - Research Process - Criteria of Good Research.

Unit – II	RESEARCH DI	ESIGN	Periods	9
Meaning of I	esearch Design - Need for Research D	esign - Features of a Goo	d Design - Im	portant Concepts
Relating to R	search Design - Different Research De	÷	of Experiment	al Designs.
Unit – III	DATA COLLEC		Periods	9
	n: Collection of Primary Data - Obse			
	ionnaires - Collection of Data throu			
	ollection of Secondary Data - Processi	ng Operations - Elements	s/Types of Ana	alysis - Statistics in
Research.	I			
Unit – IV	DATA ANALYSIS AND IN		Periods	9
	- Statistical techniques and choose			
Hypothesis to	ting - Data processing software (e.g. S	SPSS etc.) - statistical infe	erence - Interp	retation of results.
Unit - V	REPORT WRI	TING	Periods	9
Types of re	arch report: Dissertation and Thesis	s, research paper, review	v article, sho	rt communication,
conference p	esentation etc., Referencing and reference	encing styles, Research Je	ournals, Index	ing and citation of
Journals, Inte	lectual property, Plagiarism.			
]	Fotal Periods	45
References				
	R. Kothari, "Research Methodolog	y – Methods and Techr	niques", 2nd	Edition, New Age
]	ternational Publishers			
	ordens, K. S. and Abbott, B. B., "Rea	search Design and Metho	ods – A Proce	ess Approach", 8th
1	lition, McGraw-Hill, 2011			
`	obert P. Merges, Peter S. Menell, Mar	k A. Lemley, "Intellectua	ll Property in I	New Technological
	ge", 2016.		1. D	
4	avis, M., Davis K., and Dunagan N	M., "Scientific Papers a	ind Presentati	ons", 3rd Edition,
	sevier Inc.			
E-Resources				
1. <u>I</u>	tps://www.oreilly.com/library/view/re	search-methodology/9789	9353067090/	
2. 1	tps://bbamantra.com/research-method			

VLS		VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOM (Autonomous Institution, Affiliated to Anna University ,Chennai) Elayampalayam, Tiruchengode – 637 205 M.E Programme Code 205 Regulation											www.tow.com ID 9105049155			
	VLSI DESIGN / ELECTRONICS AND												23			
COMMUNICATION ENGINEERING Semester Periods Per Week Credit Ma																
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At the											Know	ledge	Level			
CO1:Describe about the concept of programme design through													Kilowiedge Level K2			
CO2: Demonstrate the practice of innovative teaching methodology													K2			
-	87	K2 K4														
CO4	CO4: Examine the infrastructure in the class room															
CO5:Define the directions of future research													K3			
-																
/1 indica	ates stro	ength of	f correla	tion) $\overline{3}$ -	Strong,		dium,	1 - Weak			Марр					
DO 2	DO 3		U			· · ·			BO			BEO	DEO			
PO 2	PO 3	PO 4	PO 5	PU 6	PO /	PU 8	POS	10 PO	PO 11			2 2	PSO 3			
		2									[
5	$\frac{3}{2}$	2						2	$\frac{2}{2}$	$\left \right $						
3			1		-		_	2	4				1			
	The I •	The main of The main of Un Un Un Ela At the end of CO1:Descri- evidences CO2:Demo CO3:Evalut CO4:Exam CO5:Defin - Y1 indicates str PO 2 PO 3 3 3 3 3 3 3	The main objective • Understan • Illustrate • Analyze th • Enhance te • Elaborate At the end of the c CO1:Describe abore cO1:Describe abore evidences CO2:Demonstrate CO3:Evaluate the CO3:Evaluate the CO5:Define the d - - /1 indicates strength of 3 3 3 3 3 3 3 3 3 3 3 3	Understand the co Illustrate the prace Analyze the meth Enhance the infra Elaborate the direct At the end of the course, t CO1:Describe about the co evidences CO2:Demonstrate the pr CO3:Evaluate the method CO4:Examine the infrast CO5:Define the direction - CO / Pe 1 indicates strength of correla Program PO 2 PO 3 PO 4 PO 5 3 3 2 3 3 2 3 3 2	The main objective of the course • Understand the concept of • Illustrate the practice of • Analyze the method of te • Enhance the infrastructure • Elaborate the directions of At the end of the course, the stude CO1:Describe about the concept evidences CO2:Demonstrate the practice of CO3:Evaluate the method of teac CO4:Examine the infrastructure CO5:Define the directions of fut - You and a strength of correlation of the strength of correlation of the strength of a streng	The main objective of the course is • Understand the concept of programe • Illustrate the practice of innovation • Analyze the method of teacher efficiency • Enhance the infrastructure in the • Elaborate the directions of future At the end of the course, the student show CO1:Describe about the concept of programe evidences CO2:Demonstrate the practice of innovation CO3:Evaluate the method of teacher edu CO4:Examine the infrastructure in the CO5:Define the directions of future reserver - Programme Outcomes PO2 PO3 PO4 PO5 PO6 PO7 3 3 2 3 3 2 3 3 2 3 3 2	The main objective of the course is • Understand the concept of programme • Illustrate the practice of innovative te • Analyze the method of teacher educatio • Enhance the infrastructure in the class • Elaborate the directions of future resear At the end of the course, the student should be a CO1:Describe about the concept of programme evidences CO2:Demonstrate the practice of innovative t CO3:Evaluate the method of teacher education CO4:Examine the infrastructure in the class ro CO5:Define the directions of future research - /1 indicates strength of correlation) 3-Strong, 2 – Me Programme Outcomes (POs) PO 2 PO 3 PO 4 PO 5 PO 6 PO 7 PO 8 3 3 2	The main objective of the course is • Understand the concept of programme design • Illustrate the practice of innovative teaching • Analyze the method of teacher education. • Enhance the infrastructure in the class room • Elaborate the directions of future research At the end of the course, the student should be able to CO1:Describe about the concept of programme design evidences CO2:Demonstrate the practice of innovative teachin CO3:Evaluate the method of teacher education CO4:Examine the infrastructure in the class room CO5:Define the directions of future research - CO/PO Mapping /1 indicates strength of correlation) 3-Strong, 2 – Medium, Programme Outcomes (POs) PO2 PO3 PO4 PO5 PO6 PO7 PO8 PO5 3 3 2	The main objective of the course is • Understand the concept of programme design through • Illustrate the practice of innovative teaching method • Analyze the method of teacher education. • Enhance the infrastructure in the class room. • Elaborate the directions of future research At the end of the course, the student should be able to CO1:Describe about the concept of programme design throug evidences CO2:Demonstrate the practice of innovative teaching method CO3:Evaluate the method of teacher education CO4:Examine the infrastructure in the class room CO5:Define the directions of future research - CO1:Describe about the concept of programme design throug evidences CO2:Demonstrate the practice of innovative teaching method CO3:Evaluate the method of teacher education CO4:Examine the infrastructure in the class room CO5:Define the directions of future research - - - - - - - - - - - - - - -	The main objective of the course is • Understand the concept of programme design through evide • Illustrate the practice of innovative teaching methodolog • Analyze the method of teacher education. • Enhance the infrastructure in the class room. • Elaborate the directions of future research At the end of the course, the student should be able to CO1:Describe about the concept of programme design through evidences CO2:Demonstrate the practice of innovative teaching methodolo CO3:Evaluate the method of teacher education CO4:Examine the infrastructure in the class room CO5:Define the directions of future research - - CO / PO Mapping 1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak Programme Outcomes (POs) PO 2 PO 3 PO 4 PO 5 PO 6 PO 7 PO 8 PO 9 PO PO 3 3 2	The main objective of the course is Interval of the course is Understand the concept of programme design through evidences. Illustrate the practice of innovative teaching methodology. Analyze the method of teacher education. Enhance the infrastructure in the class room. Elaborate the directions of future research At the end of the course, the student should be able to CO1:Describe about the concept of programme design through evidences CO2:Demonstrate the practice of innovative teaching methodology CO3:Evaluate the method of teacher education CO4:Examine the infrastructure in the class room CO4:Examine the infrastructure in the class room CO5:Define the directions of future research - PO2 PO3 PO6 PO7 PO PO PO 10 11 3 3 3 2 2	The main objective of the course is • Understand the concept of programme design through evidences. • Illustrate the practice of innovative teaching methodology. • Analyze the method of teacher education. • Enhance the infrastructure in the class room. • Elaborate the directions of future research At the end of the course, the student should be able to CO1:Describe about the concept of programme design through evidences CO2:Demonstrate the practice of innovative teaching methodology CO3:Evaluate the method of teacher education CO4:Examine the infrastructure in the class room CO5:Define the directions of future research - * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *	The main objective of the course is Interval of the course is Understand the concept of programme design through evidences. Illustrate the practice of innovative teaching methodology. Analyze the method of teacher education. Enhance the infrastructure in the class room. Elaborate the directions of future research At the end of the course, the student should be able to Colspan="2">Knowledge C01:Describe about the concept of programme design through evidences CO2:Demonstrate the practice of innovative teaching methodology K2 CO3:Evaluate the method of teacher education K4 CO4:Examine the infrastructure in the class room K3 CO/PO Mapping Yorgramme Outcomes (POs) Yo Programme Outcomes (POs) PSO PSO PSO PSO PO PO PO PO PO PO PO PO PO PSO PSO PSO PO PO PO PO PO PO PO PSO PSO PSO			

Introduction and Methodology: Aims and rationale, Policy background, Conceptual framework and terminology, Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions. Overview of methodology and Searching.

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Unit – l		THEMATIC OVERVIEW	Periods	9
		w: Pedagogical practices are being used by teachers in fo	rmal and info	mal classrooms in
developing	count	ries. Curriculum, Teacher education.		
Unit – I		PEDAGOGICAL PRACTICES	Periods	9
		e effectiveness of pedagogical practices Methodology f		
		cluded studies. How can teacher education (curriculum		
		uidance materials best support effective pedagogy? Theor		
•		dence for effective pedagogical practices. Pedagogic theory	and pedagogi	cal approaches.
		s and beliefs and Pedagogic strategies.		
Unit – I		PROFESSIONAL DEVELOPMENT	Periods	9
		lopment: alignment with classroom practices and follow-u		
		the community. Curriculum and assessment Barriers to lear	ming: limited 1	resources and large
class sizes.			1	
TI	K 7	DECEADOU CADE AND EUTUDE DIDECTIONS	Dominada	0
Unit - V	V	RESEARCH GAPS AND FUTURE DIRECTIONS	Periods	9
Research g	gaps an	d future directions, Research design, Contexts, Pedagogy		
Research g	gaps an	d future directions, Research design, Contexts, Pedagogy Dissemination and research impact.	, Teacher edu	cation, Curriculum
Research g and assessm	gaps an nent, I	d future directions, Research design, Contexts, Pedagogy Dissemination and research impact.		
Research g	gaps an nent, I s	d future directions, Research design, Contexts, Pedagogy Dissemination and research impact.	, Teacher edu Fotal Periods	cation, Curriculum 45
Research g and assessm	gaps an nent, I s Acke	d future directions, Research design, Contexts, Pedagogy Dissemination and research impact.	, Teacher edu Fotal Periods	cation, Curriculum 45
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Course (Code		Cou	ırse Na	me	F	Periods L	Per V T	Veek P		redit C	(Ma CA	ximun ES	n Mark E	s Total
P23AC	:003	Disa	aster N	Ianage	ment		2	0	0		0]	100	-		100
Course Objective	2	•	reduc Critic pract Deve relev Critic appro	n to d ction ar cally e cice fron elop an rance in cally u oaches, try or th	nd hum valuate m multi n under specif underst planni	anitaria disast iple per rstandin ic types and th ng and	in respo er risk rspectiv ng of s of dis ne stre progra	onse. redu ves. stand asters ngths mmir	ards ards and c and	and of h confl	d hun numar lict sit	nanita nitaria tuatio sses	urian n n resp ns. of di	espon ponse saster	se pol and j mana	icy ar practic
Course Outcome		CO2 CO2 CO2	1:Unde 2:Analy 3:Disas 4:Risk	of the constant the constant the constant of t	he effect ferences nageme ement t	ets of di s betwe ent tech echniqu	saster en disa niques ues	sters	and h		ds			Knov	wledge K2 K2 K3 K3 K4	Level
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CO 1	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO	8 PC)9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1 CO 2					2	2	2					2	1			
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CO 4					2	2	2					2	1			
CO 5					2	2	2					2	1			
Course As Direct				ent Tes	t I, II &	III										

Content of the syllabus Unit - I

INTRODUCTION

9

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Periods

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Introduction Di	saster: Definition, Factors and Significance; Difference	Retween Haz	ard and Disaster
	made Disasters: Difference, Nature, Types and Magnitude.	Detween maz	and and Disaster,
Unit – II	REPERCUSSIONS OF DISASTERS AND HAZARDS	Periods	9
Repercussions of	Disasters and Hazards: Economic Damage, Loss of Human	and Animal I	ife, Destruction of
Ecosystem. Natu	al Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis	s, Floods, Droi	ights and Famines,
Landslides and A	valanches, Man-made disaster: Nuclear Reactor Meltdown	, Industrial Ac	cidents, Oil Slicks
and Spills, Outbr	eaks of Disease and Epidemics, War and Conflicts.		
Unit – III	DISASTER PRONE AREAS IN INDIA	Periods	9
	reas in India Study of Seismic Zones; Areas Prone to Floo		
	as Prone to Cyclonic and Coastal Hazards with Special Refe	erence to Tsur	ami; Post-Disaster
Diseases and Epi			
Unit – IV	DISASTER PREPAREDNESS AND MANAGEMENT PREPAREDNESS	Periods	9
Disaster Prepare	lness and Management Preparedness: Monitoring of Phen	omena Trigge	ring A Disaster or
Hazard; Evaluati	on of Risk: Application of Remote Sensing, Data from Me	teorological ar	d Other Agencies,
Media Reports: C	overnmental and Community Preparedness.	-	-
Unit – IV	RISK ASSESSMENT	Periods	9
Risk Assessmen	Disaster Risk: Concept and Elements, Disaster Risk I	Reduction, Glo	obal and National
	tuation. Techniques of Risk Assessment, Global Co-Ope		
	's Participation in Risk Assessment. Strategies for Surviva		
	ategies of Disaster Mitigation, Emerging Trends in Mitig	ation. Structu	ral Mitigation and
Non-Structural M	litigation, Programs of Disaster Mitigation in India.		
	r 	Fotal Periods	45
References			
	shith, Singh AK, "Disaster Management in India: Perspect	ives, issues an	d strategies "'New
Roya	l book Company.		
	i, Pardeep et.al. (Eds.)," Disaster Mitigation Experiences a	nd Reflections	", Prentice Hall of
India	Now Dolh		
	, New Delhi.		
3 Goel	S. L., Disaster Administration and Management Text Ar cation Pvt. Ltd., New Delhi.	d Case Studie	es", Deep & Deep
3 Goel	S. L., Disaster Administration and Management Text Ar	nd Case Studio	es", Deep & Deep
3. Goel Publi	S. L., Disaster Administration and Management Text Ar		es", Deep & Deep

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Prog	gramme	M.	E				Prog	ramm	e Code	2	205	Reg	ulatior	1	202	23
Dep	artment				ELECT							Se	emester	r		
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P23A	C004	Val	ue Edu	ication			2	0	0	(0		100	-		100
Course Objectiv	ve	The	To in To in To e To d	ntroduc nterpre laborat listingu	ve of the e the va t good v e the imp uish the	lue of values portan relati	educa in stuc ce of c onshi	dents. charac p anc	eter. I their							
Course Dutcom	le	 To interpret the religions and equality. At the end of the course, the student should be able to CO1:Understand education values CO2:Analyze importance of cultivation values CO3:Importance of personality development 											Knov	vledge K2 K2 K3	Level	
		CO	CO4:Character maintenance												K3	
			CO5: Examine the religions and honesty. K4													
Pre-requence of Cos			cates str	ength of	CO / PC f correlat Program	ion) 3-	Strong			, 1 - `	Weak			CO/I Map PSOs	ping	
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO	8 PO	9	PO	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1	3	3	3	2							10	11	12	1	2	3
CO 2	3	3	3	2												
CO 3	3	3	3	2				_								
CO 4 CO 5	3 3	3 3	3	2 2												
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1.	Course of the st															
Unit Values	of the sy t - I and sel m. Mora	f-deve	elopme			lues a	and ir	ndivid				Work		, Ind	9 ian vi	sion (
							~2	e Su		_		7				56

Unit – II	IMPORTANCE OF CULTIVATION OF VALUES	Periods	9
Importance of	cultivation of values. Sense of duty. Devotion, Self-relia	nce. Confider	ice, Concentration.
Truthfulness, (Cleanliness. Honesty, Humanity. Power of faith, National Un	nity. Patriotisn	n. Love for nature,
Discipline.		-	
Unit – III	PERSONALITY AND BEHAVIOR	Periods	9
Unit – III	DEVELOPMENT	renous	7
Personality an	d Behavior Development - Soul and Scientific attitude. I	Positive Think	ting. Integrity and
discipline. Pun	ctuality, Love and Kindness. Avoid fault Thinking. Free from	anger, Dignity	of labour.
Unit – IV	RELATIONSHIP MANAGEMENT	Periods	9
Universal broth	erhood and religious tolerance True friendship. Happiness Vs	suffering, lov	e for truth.
Aware of self-	lestructive habits. Association and Cooperation. Doing best fo	r saving nature	e.
Unit - V	CHARACTER AND COMPETENCE	Periods	9
Character and	Competence -Holy books vs Blind faith. Self-management	nt and Good	health. Science of
reincarnation.	Equality, Nonviolence, Humility, Role of Women. All religion	ns and same m	nessage. Mind your
Mind, Self-cor	trol. Honesty, Studying effectively.		
	, , , , , , , , , , , , , , , , , , ,	Fotal Periods	45
References			
1. C	hakroborty, S.K. "Values and Ethics for organizations Theory	and practice",	, Oxford
1. U	niversity Press, New Delhi 2011.	•	
E-Resources			
1. h	tps://www.ncbi.nlm.nih.gov/pmc/articles/PMC5132380/		
<u> </u>	tps://www.examrace.com/Study-Material/Education/Value-	lucation-You7	Tube-Lecture-
2. H	andouts.html		

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		KANANDHA COLI Autonomous Institution Elayampa	n, Affili	ated to	Anna	Universi	ty ,Chennai)	τί	VEnerinard Wenerinard Beneficion D structure D structure	
Programme	M.E		Pro	gramm	e Code	205	Regulation		2023	
Department		ESIGN / ELECTRO					Semester			
Course Code	(Course Name	Period	ls Per T	Week P	Credit C	Maxi CA	ximum Marks ESE Total		
P23AC005	L I I C C/I Constitution of India2000100							-	100	
Course Objective	 To To co er To Ro To To 	in objective of the co o understand the pren vil rights perspective. o identify the growt onstitutional role and nergence of nationhoo o illustrate the role of evolution and its impa o categorize the gov o interpret the vario	h of In h of In l entitle od in the f sociali act on the ernance us adm	dian o ement e early sm in ne initi e bodi inistra	opinion to civi years c India a: al draft es in th ation in	regardin and e of Indian fter the c ing of the ne organ a states.	ng modern In conomic righ nationalism. commencement e Indian Cons ization.	ndian ir nts as v nt of the stitution.	ntellectuals' vell as the e Bolshevik	
Course Outcome	CO1: D CO2: C CO3:Ur CO4:De	nd of the course, the s efine the history of In ategorize the important inderstand the function emonstratethegovernation ioritize the local and c	dian Co nce of c is of Loo nce bod	onstitut onstitu cal adr ies in	ion itional r ninistra the orga	ights and tion anization	1 duties.		dge Level K2 K3 K2 K4 K4	
Pre-requisites							-			

	CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak														
Cos	Programme Outcomes (POs)													:	
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO	PSO 2
CO 1	3	3	2	2						10	11	12	1	4	3
CO 2	2	2	2	2											
	3	3	Z	Z											
CO 3	3	3	2	2											
CO 4	3	3	2	2											
CO 5	3	3	2	2											

Direct

- 1. Continuous Assessment Test I, II & III
- 2. Assignment and Seminar

Indirect

1. Course - end survey

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Unit - I	INTRODUCTION	Periods	9
History of Makir	g of the Indian Constitution: History Drafting Committee, (Composition &	z Working)
Unit – II	PHILOSOPHY OF THE INDIAN CONSTITUTION	Periods	9
Philosophy of the	Indian Constitution: Preamble, Salient Features		
Unit – III	CONTOURS OF CONSTITUTIONAL RIGHTS & DUTIES	Periods	9
Contours of Con	stitutional Rights& Duties: Fundamental Rights- Right to Eq	uality- Right to	Freedom
Right against E	xploitation- Right to Freedom of Religion ,Cultural and	d Educational	Rights, Right to
Constitutional Re	medies, Directive Principles of State Policy, Fundamental D	Duties	
Unit – IV	ORGANS OF GOVERNANCE	Periods	9
	nance: Parliament, Composition, Qualifications and Disqual		
	dent, Governor, Council of Ministers, Judiciary, Appoint	tment and Tr	ansfer of Judges,
Qualifications, P	owers and Functions.		
Unit - V	LOCAL ADMINISTRATION	Periods	9
	ation: District's Administration head: Role and Important		
Mayor and role	of Elected Representative, CEO of Municipal Corporation.	Pachayati raj:	Introduction, PRI:
	lected officials and their roles, CEO ZilaPachayat: Po		
	ierarchy (Different departments) Village level: Role of Elect	ted and Appoir	ted officials,
Importance of gr	ass root democracy		
		Fotal Periods	45
References			
1. The	Constitution of India, 1950 (Bare Act), Government Publicat	ion.	
2. Dr. S	. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution	on, 1 st Edition,	2015.
3. M. P	. Jain, Indian Constitution Law, 7th Edition., Lexis Nexis, 20	014.	
E-Resources			
			1 DD 1 C
1. http	s://nptel.ac.in/courses/129/106/129106002/ CO-ORDINATE		ADRAS

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WOMEN ENPO				nomous	Institut	tion, At	ffiliate	d to A	nna U	RING F niversity 637 205	,Che		EN	TÜVRheinland CERTIFIED	9 9001-2015		
Prog	gramme	M.I	E		Prog	gramme	e Code			205	R	egulat	ion	20)23		
Dep	artment				ELEC ION E							Semes	ster				
Course	e Code		Cou	ırse Na	me		eriods L	Per V T	Veek P	Credit C		Ma CA		n Mark ESE	ts Tota		
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					ve of th	e cours	e is										
		•		•				ng sk	ills and	l level o	f read	ability	,				
Course		•			to write			-				5					
Objectiv	ve	•															
- SJeen		•							U		hmiaa	ion					
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		•				-	-			omissior	of pa	iper.	**		-		
		At the end of the course, the student should be able to											Knov	vledge			
Course		CO1: Understand forming and brake up sentences.											K2				
Jourse Dutcom	le		CO2:Importance of finding plagiarism.											K4			
, accom			CO3: Summarize the concept of literature reviews.K2CO4: Extend the focus on chill development estivitiesK2														
			CO4: Extend the focus on skill development activities.K2CO5: Develop the writing skills in the paper.K3														
Pre-requ		CO5	: Dev	elop the	e writing	g skills :	tills in the paper. K3										
Cos				ength of	CO / PO f correla Program PO 5	tion) $\overline{3}$ -	Strong, comes	(POs)		1 - Weal		PO	CO/I Map PSOs	ping	- DSO		
	PO 1	PO 2	PO 3	PO 4	PO 5	PU 6	PO 7	POS	B PO	9 PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3		
CO 1	3		3	2													
CO 2 CO 3	3	3	3 3	2											+		
	3		3	2					+								
CO 4	3		2	2													
CO 4 CO 5	5																
	5																
CO 5	Assessme	ent Me	thods														
CO 5		ent Me	thods														
CO 5 Course A	Assessm Continu	ious As	ssessm		t I, II &	III											
CO 5 Course A Direct 1. 2.	Assessm Continu Assigni	ious As	ssessm		t I, II &	III											
CO 5 Course A Direct 1. 2. Indirec	Assessm Continu Assigni	ious As ment an	ssessm nd Serr		t I, II &	III											
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CO 5 Course A Direct 1. 2. Indirect 1. Content Unit Planning	Assessm Continu Assign ct Course	ious As ment an - end si yllabus eparati	ssessm nd Sem urvey s P on, W	hinar PLANN Yord Or	ING A der, Br	ND PF	up lor	ng ser	ntences		uring 1		raphs a				

Unit – II	CLARIFICATIONS	Periods	9
	o Did What, Highlighting Your Findings, Hedging and	l Criticising,	Paraphrasing and
Plagiarism, Se	ctions of a Paper, Abstracts. Introduction.		
Unit – III	LITERATURE REVIEW	Periods	9
Review of the	Literature, Methods, Results, Discussion, Conclusions, The Fin	nal Check.	
Unit – IV	SKILL DEVELOPMENT - I	Periods	9
•	needed when writing a Title, key skills are needed when writing an Introduction, skills needed when writing a Review of	0	
Unit - V	SKILL DEVELOPMENT - II	Periods	9
Skills are need	ed when writing the Methods, skills needed when writing the	Results, skill	s are needed when
writing the Dis	cussion, skills are needed when writing the Conclusions, useful	ıl phrases, hov	v to ensure paper is
as good as it co	ould possibly be the first- time submission		
		Total Period	ls 45
References			
1. Go	ldbort R (2006) Writing for Science, Yale University Press (av	vailable on Go	ogle Books)
2. Da	y R (2006) How to Write and Publish a Scientific Paper, Cam	bridge Univers	sity Press
	rian Wallwork, English for Writing Research Papers, Sidelberg London, 2011	Springer New	V York Dordrecht
E-Resources			
1. h	tps://nptel.ac.in/courses/110/105/110105091/ CO-ORDINATI	ED BY : IIT K	HARAGPUR
2. h	tps://www.udemy.com/topic/research-paper-writing		

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					ve of th	e cours	e is								
				0	achieve			bal hai	opily.						
Course					person	-	-	-		g perso	nality :	and de	termin	ation	
Objectiv	ve			•	e wisdo					8 P • 180					
objecti	ve				managii				7						
				•	•	•		•	•						
		Δ++	Extend the increasing productivity. At the end of the course, the student should be able to											vladaa	Laval
			CO1: Identify goals												Level
Course			CO1: Identify goalsK2CO2:Analyze Personality developmentK2												
Outcom	e		CO2:Anaryze reisonancy developmentK2CO3:Make use of appropriate life and career goalsK3												
			CO3.Wake use of appropriate me and career goalsK3CO4: Developing relationships with othersK3												
			CO4: Developing relationships with othersKSCO5:Understand the value of diversityK2												
D	•••														
Pre-req	uisites														
			CO / PO Mapping												
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Cos	(3/2	2/1 indic	cates str	ength of	f correla	tion) $\overline{3}$ -	Strong,		edium,	1 - Wea	ık		Мар	ping	
Cos	(3/2 PO 1	2/1 india	cates str	ength of		tion) $\overline{3}$ -	Strong,				lk PO	РО		ping	PSO
	PO 1	PO 2	PO 3	PO 4	f correla Program	tion) 3-3 me Out	Strong, comes ((POs)	PO			PO 12	Map PSOs	ping	PSO 3
CO 1	PO 1 3	PO 2 3	PO 3	PO 4	f correla Program	tion) 3-3 me Out	Strong, comes ((POs)	PO 2	9 PO	РО	-	Map PSOs PSO	ping S PSO	
	PO 1 3 3	PO 2 3 3	PO 3	PO 4 2 2 2	f correla Program	tion) 3-3 me Out	Strong, comes ((POs)	PO	9 PO	РО	-	Map PSOs PSO	ping S PSO	
CO 1 CO 2	PO 1 3	PO 2 3	PO 3 3 3	PO 4	f correla Program	tion) 3-3 me Out	Strong, comes ((POs)	PO 2 2	9 PO 10	РО	-	Map PSOs PSO	ping S PSO	
CO 1 CO 2 CO 3	PO 1 3 3 3 3	PO 2 3 3 3	PO 3 3 3 3	PO 4 2 2 2 2	f correla Program	tion) 3-3 me Out	Strong, comes ((POs)	PO 2 2	9 PO 10 2	РО	-	Map PSOs PSO	ping S PSO	
CO 1 CO 2 CO 3 CO 4 CO 5	PO 1 3 3 3 3 3 3 3 3 3	PO 2 3 3 3 3 3 3 3	PO 3 3 3 3 3 3 3	PO 4 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	f correla Program	tion) 3-3 me Out	Strong, comes ((POs)	PO 2 2	9 PO 10 2	РО	-	Map PSOs PSO	ping S PSO	
CO 1 CO 2 CO 3 CO 4	PO 1 3 3 3 3 3 Assessn	PO 2 3 3 3 3 3 3 3 ment M	PO 3 3 3 3 3 3 6 ethods	PO 4 2 2 2 2 2 2 2 2 2 2 2 2 2	f correla Program PO 5	rion) 3-4 me Out PO 6	Strong, comes ((POs)	PO 2 2	9 PO 10 2	РО	-	Map PSOs PSO	ping S PSO	
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CO 1 CO 2 CO 3 CO 4 CO 5 Course 2 Direct 1. 2. Indirect 1. 2. Indirect 1. Verses- Verses-	PO 1 3 3 3 3 3 3 Assessn Contin Assign Course of the s t - I akam-H 19,20,2 29,31,3	PO 2 3 3 3 3 3 3 aent M muous A ment a e - end syllabu Holistic 1,22 (v 2 (prid	PO 3 3 3 3 3 3 3 ethods survey s develo visdom le & he	PO 4 2 2 2 2 2 2 2 2 2 2 2 2 2	f correla Program PO 5 t I, II &	tion) 3-s me Out PO 6	Strong, comes (PO 7	(POs) PO 8	PO 2 2	9 PO 10 2	PO 11		Map PSOs PSO	ping S PSO 2 	3
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Neetisataka	m-Holistic development of personality		
Verses- 52,	53,59 (dont's)		
Verses-71,	73,75,78 (do's)		
Unit – I	II APPROACH TO DAY TO DAY WORK AND DUTIES	Periods	9
Approach t	o day to day work and duties.		
Shrimad Bl	nagwad Geeta :		
Chapter 2-V	Verses 41, 47,48,		
Chapter 3-V	Verses 13, 21, 27, 35,		
Chapter 6-V	Verses 5,13,17, 23, 35,		
Chapter 18	-Verses 45, 46, 48.		
Unit – I	V STATEMENTS OF BASIC KNOWLEDGE	Periods	9
Statements	of basic knowledge.		
Shrimad Bl	nagwad Geeta:		
Chapter2-V	Verses 56, 62, 68		
Chapter 12	-Verses 13, 14, 15, 16,17, 18		
Unit - V		Periods	9
	of Role model.		
	nagwad Geeta:		
Chapter2-V			
	Verses 36,37,42,		
-	Verses 18, 38,39		
Chapter18	– Verses 37,38,63		
		Total Periods	45
References			
1.	"Srimad Bhagavad Gita" by Swami SwarupanandaAdvaita A Kolkata	shram (Publicati	on Department),
2.	Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P.Gopina	ath,	
3.	Rashtriya Sanskrit Sansthanam, New Delhi.		
E-Resource	es		
1.	https://library.um.edu.mo/ebooks/b17771201.pdf		
2.	https://www.staticcontents.youth4work.com/university/Documerach/29f57018-6412-4dee-b24b-ac29e54a0f9e.pdf	nts/Colleges/Coll	legeSummaryAtt

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A DESCRIPTION OF THE REAL		VIV		iomous	Institut	ion, A	ffiliated	l to A	nna U	RING F niversity 637 205	,Che		EN	TÜVRheinland CERTIFIED	8001:2015		
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		CO		nine the	and pro			g in en	suring	harmon	y in sc	ociety		K3			
Pre-req	uisites																
	(3/2	/1 indic	cates str	ength of		tion) 3-	Strong,		edium,	1 - Weak	2			ping			
COs	PO 1	PO 2	PO 3	PO 4	Program PO 5	me Out PO 6	PO 7	(POs) PO 8	PO	9 PO	PO	PO	PSO PSO	s PSO	PSO		
			-						_	10	11	12	1	2	3		
201	1	1		3	3	1	2	3		3 2	3	1	<u> </u>		-		
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Direct

- 1. Continuous Assessment Test I, II & III
- 2. Assignment and Seminar

Indirect

1. Course - end survey

Former

Unit -	- I Introduction-Basic Human Aspiration	Periods	9
	human aspirations and their fulfillment through Right under		
	ding and Resolution as the activities of the Self, Self being ce		
	sing Resolution for a Human Being, its details and solution	n of problems	in the light of
Resolution			
Unit –		Periods	9
	ain of right understanding starting from understanding the h		
	er and the doer) and extending up to understanding nature/existent		
co-exister	ice; and finally understanding the role of human being in existence		ct).
Unit –	0 0	Periods	9
	ding the human being comprehensively as the first step and the c		
	co-existence of the self and the body; the activities and pote contradiction in the self	ntialities of the	self; Basis for
Unit –	IV Understanding Nature and Existence	Periods	9
A compre	hensive understanding (knowledge) about the existence, Natur	e being include	d; the need and
	f inner evolution (through self-exploration, self awareness ar		
awakenin	g to activities of the Self: Realization, Understanding and Contem	plation in the se	lf.
Unit -	V Understanding Human Conduct	Periods	9
Understar	iding Human Conduct, different aspects of All-encompassi	ng Resolution	(understanding,
	cience etc.), Holistic way of living for Human Being with Allen		
	imensions of human endeavor viz., realization, thought, behavio		ticipation in the
larger ord	er) leading to harmony at all levels from Self to Nature and entire	Existence	
		Total Periods	45
Text Books			
1.	R R Gaur, R Asthana, G P Bagaria, 2019 (2nd Revised Edition), A Foundation	Course in
1.	Human Values and Professional Ethics. ISBN 978-93-87034-4	7-1, Excel Book	s, New Delhi.
2.	Premvir Kapoor, Professional Ethics and Human Values, Khan	na Book Publisł	ing, New
	Delhi, 2022.		
۷.	Denn, 2022.		
	s E-Resources		
		er, and Harper C	Collins, USA
References	s E-Resources	<u>^</u>	
References 1.	s E-Resources Ivan Illich, 1974, Energy & Equity, The Trinity Press, Worcest E.F. Schumacher, 1973, Small is Beautiful: a study of econom & Briggs, Britain	<u>^</u>	
References 1. 2.	s E-Resources Ivan Illich, 1974, Energy & Equity, The Trinity Press, Worcest E.F. Schumacher, 1973, Small is Beautiful: a study of econom & Briggs, Britain	<u>^</u>	

		VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution, Affiliated to Anna University ,Chennai) Elayampalayam, Tiruchengode – 637 205												SO MRI 2015 TUVenahada CENTINES 0 11004000		
Progra	M.	M.E Programme Co						de		Reg	ulation	n 2023				
Depar	VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING									Semester						
Course Code		Course Name			P	Periods Per Week			Credit				num Marks			
						L	Т	Р	C		CA	ES		Total		
P23AC009			Online Course				2	0	0	0		100	-		100	
Course Objective Course Outcome Pre-requi	At the cost of the	 Understand the importance of online certification courses. Distinguish about job opportunities. Make use of this course can prepare the competitive examination. Classify the online tools for course. At the end of the course, the student should be able to CO1:Evaluate the programming skills. CO2:Identify online certifications. CO3:Appraise the value of the courses and job opportunities CO4: Categorize in Quantitative Reasoning and Technological Literacy. CO5: Develop the ICT tools for the specific course. 														
Cos	CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak												CO/PSO Mapping PSOs			
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO	8 PO	9 PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3	
CO 1	3	3	2	2				1		2						
CO 2	3	3	2	2						2						
		3	2	2						2	2					
		3	2	2						2	2					
CO 5	3	3	2	2							2					

Direct

1. Online Assignments and Assessments

Indirect

1. Course - end survey

LIST OF COURSES

Online Courses such as :

- 1. NPTEL Courses
- 2. SWAYAM Courses
- 3. IIT-B Spoken Tutorials
- 4. UDEMY Courses
- 5. CCNA Courses
- 6. MOOC Courses
- 7. Microsoft Virtual Academy Certification courses etc.,

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